Development of Signal Sources for Millimeter and Submillimeter Wave Output

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To all those who took the time to believe in me

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LIST OF SYMBOLS AND ABBREVIATIONS

$\sim$	approximately equal to
$>$	greater than
$<$	less than
B_{LOCK}	locking bandwidth
Cu	copper
dB	decibel
dB	decibels relative to carrier
dBm	decibels referenced to one milliwatt
DC	direct current
DRIE	deep reactive ion etch
EDM	electronic discharge machining
ϵ_r	dielectric constant
FET	field effect transistor
FOM	figure of merit
f_{osc}	frequency of oscillation
f_t	frequency transition - the frequency where gain falls to unity
GaAs	gallium-arsenide
GHz	gigahertz = 10^9 cycles per second
HBT	heterojunction bipolar transistor
HBV	heterostructure barrier varactor
Hz	hertz = 10^9 cycles per second
in	inches
InGAP	indium gallium phosphide
InP	indium phosphide
IL	insertion loss

ILO	injection locked oscillator
kHz	killihertz = 10^3 cycles per second
KV	killi-volts = 10^3 volts
LO	local oscillator
L_{SSB}	single sideband noise
mA	milli-ampere = 10^{-3} ampere
MHEMT	metamorphic high-electron mobility transistor
mm	millimeter = 10^{-3} meter
MMIC	monolithic microwave integrated circuit
mW	milliwatt = 10^{-3} watts
NBW	noise bandwidth
nH	nano henries = 10^{-9} henries
pF	pico farads = 10^{-12} farads
PHEMT	pseudomorphic high-electron mobility transistor
pF	femto farads = 10^{-12} farads
PLO	phase locked oscillator
P_{DC}	DC power consumption
P_{out}	output power
P_{SSB}	single sideband power
Q	quality factor
rad	radians
RBW	resolution bandwidth
RIE	reactive ion etch
RF	radio-frequency
Si	silicon
SiGe	silicon germanium
SOLT	short, open, load, and thru
STS	Surface Technology Systems
$tan\ \delta$	loss tangent

Ti	titanium
THz	terahertz = 10^{12} cycles per second
TE	transverse electric wave
TEM	transverse electromagnetic wave
TM	transverse magnetic wave
TRL	through-reflect-line
um	micron = 10^{-6} meter
VCO	voltage controlled oscillator
W-Band	75-110 GHz

SUMMARY

The objective of this research is to develop signal sources for millimeter and sub-millimeter wave. This includes a W-Band oscillator fabricated on Raytheon's metamorphic high-electron mobility transistor (MHEMT) substrate, and the development of a frequency multiplier utilizing silicon micromachining waveguide and brass waveguide blocks. The contributions from this research include the development of the first W-Band oscillator on MHEMT substrate; a unique method of injection locking for phase noise characterization; the characterization of the first silicon micromachined straight waveguide at 400 GHz; the characterization of the first silicon waveguide based multiplier utilizing an HBV diode with an output of 261 GHz; and the demonstration of increased power generation utilizing waveguide couplers and two HBV diodes with an output of 260 GHz.

The first section gives the research background and a review of current technologies related to signal generation. The various methods used to generate W-Band signals are first reviewed along with the positive and negative attributes of each approach. Then, a short review of the most popular semiconductor substrates used to generate W-Band signals is presented. Next, the two most popular types of waveguides are considered with the focus given to the rectangular waveguide. Followed by the discussion of two methods for the terahertz (THz) signal generation, especially on the RF/microwave generation method. Lastly, a review of the alternative methods to form the rectangular waveguides including the use of: SU-8 photoresist, wet etching of silicon, dry etching of silicon, and laser etching of silicon.

The first research topic revolves around the development of a W-Band oscillator using Raytheon's MHEMT substrate. Two different design approaches, a common gate and common source, are extensively covered along with the excellent results. Furthermore, a unique method of injection locking for phase noise measurement is presented.

The second research topic discusses the signal generation toward THz signal. The first topic is the development of a silicon micromachined waveguide at 400 GHz. The extensive analysis on the packaging of the silicon waveguide is demonstrated and the results are shown. The dissertation then continues the use of the silicon micromachined waveguide in a multiplier application with the output frequency of 261 GHz. The fabrication, assembly and results of the first micromachined waveguide based multiplier utilizing an HBV diode are covered, which demonstrates the viability of using silicon micromachined waveguide in place of regular machined waveguide. Finally, a method of generating more output power utilizing the same HBV diode circuits is demonstrated. A power combiner block is developed using two waveguide branchline couplers for the power dividing and combining, respectively, in order to generate a larger amount of output power than with a single multiplier.

CHAPTER I

INTRODUCTION

1.1 Signal Generation

Since the dawn of electronic circuits, a signal source to help operate those circuits has been an important component. The birth of wireless telecommunications advanced the need for a signal source, commonly referred to as a local oscillator (LO). LO sources are found in nearly every piece of electronic equipment today. High-performance, off-the-shelf LO sources are available for a host of applications, but as higher frequencies are utilized, these components have become impractical and not readily available. LO sources are required, typically integrated into the system that requires the source. This research focuses on custom sources, the development of a W-band, on-wafer LO source, and the implementation of a multiplier for use in a signal source chain for THz circuits, using micromachined silicon to form the waveguide.

1.2 W-Band Sources

While vacuum tubes can be used for W-band sources, these sources are typically composed of solid state devices, generally using a GaAs based substrate. The active device is either a diode or transistor. Two methods of generating a W-band signal are generating at a lower frequency source and multiplying up to the desired frequency (often referred to as a source module) or directly generating the fundamental signal.

A source module is attractive because it can be composed of multiple types of technologies that have the potential to deliver excellent performance compared to a single technology. Typically, these configurations use a much lower starting frequency that utilizes a higher Q resonator, such as a dielectric resonator or a crystal resonator. This can yield better performance in terms of phase noise and frequency stability. The starting frequency is then sent through a chain of multipliers (and amplification stages if desired) until the desired

frequency is achieved. While this approach has the potential to produce superior results, it can be cost prohibitive from the standpoint of integration and assembly. The multiplication approach can also be achieved by using one type of technology.

Direct generation of the fundamental frequency requires many fewer components to generate the actual signal; thus, it will use significantly less surface area of a wafer. It is possible to phase lock a direct generation approach. However, the conversion loss associated with dividing down the fundamental frequency is appreciable. Because chip area is a concern, direct generation of W-band signal is suitable when frequency stability is not a primary concern.

When considering frequency stability, there are two popular approaches used to achieve very high stability: injection-locked oscillators and phase-locked oscillators. Injection-locked oscillators (ILOs) are direction-generation oscillators that are stabilized by injecting a subharmonic frequency into the direction-generation oscillator. One factor that impacts the quality of the result is the cleanliness of the injection locking signal, which directly affects the phase noise of the direct-generation signal [33]. While this necessitates the generation of a lower frequency signal to perform the injection lock, either on- or off-wafer, it typically requires a relatively low power level to achieve the lock. Consequently, filtering the subharmonic signal at the output is often not necessary. One disadvantage of this approach can be the small locking range of the oscillator, which will limit the range of a VCO application, particularly when using a higher subharmonic signal (4th, 5th, etc.) [70].

Phase-locked oscillators (PLOs) generally provide the best performance available in terms of phase noise and frequency stability. There are essentially two ways to achieve a PLO: by phase locking a lower signal source and multiplying up to the desired frequency or by dividing (often called a prescaler) a direct-generation frequency. The latter can be difficult to achieve when frequency goes up, as prescalers or dividers become very lossy. A PLO approach is generally the most expensive type of configuration because of the required components: a VCO, mixer, and phase comparator.

1.3 W-Band Substrates

There are multiple substrates available for W-band active circuitry. The dominant substrates available today consist of GaAs, InP, and various GaAs-based compounds such as PHEMT and MHEMT. SiGe and GaN are quickly becoming competitors in the W-band area.

InP, or indium phosphide, is the gold standard for W-band and higher frequency circuitry with regard to output power and noise performance [59]. An InP HEMT is currently the best non-module power amplifier at 95 GHz, with a record setting 427 mW of output power with a 19% efficiency [13]. The great advantage of InP is its very high electron mobility and high breakdown voltage, which make it well suited for high-speed and high breakdown voltage electronic applications. InP also boasts the highest f_T frequencies and is used in applications into the low THz frequency range. Despite all these positives attributes, InP-based circuits have been limited by their fragility, small wafer size, and low yield InP substrates, resulting in a high cost per circuit and poor reliability [22].

SiGe, or silicon germanium, is rapidly developing into a very viable platform for W-band circuitry. IBM's SiGe HBT 8T process currently boasts f_T=207 GHz [53]. And IBM's most recent SiGe process, 9T, has an f_T=350 GHz [56]. SiGe has great properties in terms of noise performance for oscillators because it is superior 1/f and phase noise. More recent publications reported SiGe oscillators operating in the W-band range and at 190 GHz, demonstrating SiGe viability at very high frequencies [62, 63].

GaN, or gallium nitride, has been know for high power applications since it can operate with much higher voltages, but has been limited to frequencies below 50 GHz due difficulty with processing. Recently, the operating frequencies of GaN have been pushed into the low W-band range [24, 51]. A recent power amplifier application generated an output power of 316 mW at 80.5 GHz [46]. This accomplishment in the inital stages of development rivals that if InP and shows promise to eclipse InP's power performance as the technology is improved.

The PHEMT substrate followed the development of GaAs and provides superior performance in terms of very low noise and high power / high efficiency at very high frequency

ranges. The PHMET substrate has, in recent years, been the substrate of choice for W-band oscillator development because of its noise properties [8, 12, 34, 54, 61].

The MHEMT substrate has recently begun to mature for use in the W-band frequency range. MHEMT provides the low noise characteristic and power characteristics similar to those of InP, but it is a much more manufacturable product than InP [47]. It is also able to be fabricated on 4" and 6" wafers compared to InP 3" wafers. Raytheon, Inc. has demonstrated the power capabilities of the MHEMT substrate with a recent single-stage power amplifier with 267 mW output power. This has set the stage for this MHEMT process to now rival InP in the area of high-power amplifiers [22, 23, 36].

It is generally accepted that HBTs are more attractive in oscillator applications compared to FET devices because a low flicker noise corner frequency. In addition, InGAP, GaAs, and SiGe HBTs have been shown to have superior 1/f noise performance compared to FET devices [70].

A list of the most recently published monolithic W-band oscillators is shown Table 1 with their associated performance.

Table 1: A sample of recent oscillator performance. Listed is the year of publication, device type used, frequency of operation (GHz), output power (dBm) and phase noise at a 1 MHz offset from the carrier (dBc/Hz).

Reference	[8]	[34]	[30]	[6]	[57]	[35]	[66]
Year	1996	1998	1999	2000	1999	2004	2005
Device	PHEMT	PHEMT	InP HBT	InP HBT	InGaP HBT	GaAs HBT	SiGe
Frequency(GHz)	94	94	108	94	104	73	82
Output Power(dBm)	7.78	2	0.92	-3	-3.4	0	3.9
Phase Noise(dBc/Hz)	-67	-71	-88	-85	-95	-100	-105

1.4 Waveguide

One of the most unique transmission mediums for microwave frequencies is waveguide. Waveguide can take variations of multiple forms, but the two most popular are rectangular and circular. The primary unique property of waveguide is its use of a single conductor for transmission. This fact allows no conduction of DC current or voltage, nor does it allow

the propagation of TEM signals. Multiple modes are possible in both types of guides, with each mode having a different cutoff frequency. An example of a rectangular waveguide (left) and an example of a circular waveguide (right) is shown in Figure 1. Both of these types of guides have cutoff frequencies below which no signal will propagate. While both of these guides are useful, rectangular waveguide has received more attention toward development since its inception. Extensive research was carried out by the MIT Radiation Lab during World War II and culminated into a 27 volume set on radar work, including a microwave handbook by Marcuvitz [43].

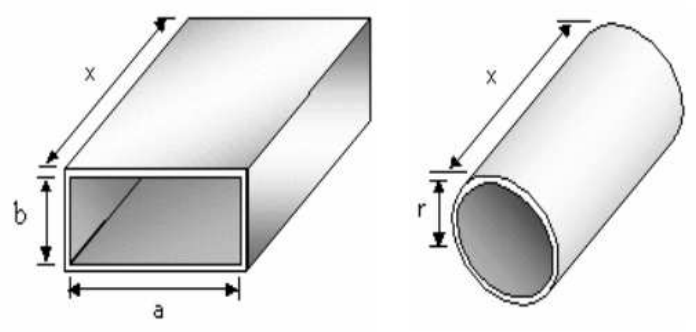

Figure 1: Example of a rectangular waveguide (left) and a circular waveguide (right).

Rectangular waveguide is defined primarily by its dimensions. Its 'a' dimension is long wall or broad wall and its 'b' dimension is the short wall or height, as shown in Figure 1. Generally, a relationship of b=0.5*a is maintained for standardized dimensions. Standard rectangular waveguide sizes exist for frequencies from 0.32 GHz up to 325 GHz. These sizes are broken up into multiple sizes that are assigned a useable bandwidth, designated by a WR-XXX standard number. Beyond 325 GHz, there exists no standardized dimensions, but a formula is generally followed where the inner a dimension is set to the WR number divided by 100. For example, WR-2 would have an 'a' dimension of 0.02 in and a corresponding 'b' dimension of 0.01 in. Defining the usable frequency ranges is established by calculating the first two modes that can be present in rectangular waveguide. The primary mode is TE_{10} and the next mode is TE_{20}. The formula used to calculate cutoff frequencies is:

$$f_{c_{mn}} = \frac{c}{2 * \pi} \sqrt{\left(\frac{m * \pi}{a}\right)^2 + \left(\frac{n * \pi}{b}\right)^2} \tag{1}$$

where a and b are the waveguide dimensions, c is the speed of light, and m and n are the order of the TE or TM modes.

Multiple fabrication methods currently exist for waveguide. For standard simple waveguide structures, stock waveguide can be used and formed into the necessary shapes attaching the necessary flange pattern by welding. One alternative is electro-forming. In this process, an entire waveguide structure is built up by electroplating, then the desired structure is burned out, leaving the waveguide. This works well for complex structures, but is very time consuming and expensive. Dip-brazing is another technique of joining stock waveguide, but it not suitable for high frequencies as the waveguide can become deformed during the process. Another method in use is electronic discharge machining waveguide or EDM. EDM can be performed using two techniques: wire EDM and plunge EDM. Both methods use a high amount of voltage to melt away the desired metal pattern. Both techniques can be accurate to one mil or less. A more common method employs a standard milling technique with computer control, called CNC milling. This method can be extremely accurate as the milling is computer controlled, but can be limited to less complicated shapes that may be desired. There are also numerous efforts in developing the use of a laser system that can cut complex metal shapes to form waveguides.

1.5 THz signals

Terahertz (THz) frequencies are gaining more attention due to their unique properties. A host of applications such as biological and chemical weapons detection, in place of airport metal detectors and other traditional weapons screening tools [4]. There is significant promise in using THz frequencies for medical imaging, since these frequencies are non-ionized radiation and will not cause skin damage as is possible with X-ray technology. However, water is an obstacle to THz radiation; thus, THz signals are currently best suited for medical applications that do not require deep penetration, such as skin cancer analysis or dental examination [5, 15].

Successful uses of THz signals are predominantly found in space-born applications, as this avoids the water in the atmosphere. One popular set of data that comes from THz

signal has to do with the theory of global warming, that includes the detection of the many types of chemicals present in the upper atmosphere. THz sensors can yield significant information from distant objects in space such as other planets or distant galaxies [42].

When considering Terahertz (THz) signal generation, there are two distinctive ways to generate the signal: by laser, or by RF/Microwave generation. Laser systems are much more mature at generating THz signals. The lower limits of laser based system are constantly being pushed and some reach down towards 0.1 THz. However, these lasers are generally very large, despite their constantly improving technology, which limits their potential applications where small size and light weight are needed.

A traditional RF approach to these signals can provide some significant advantages over laser-based generation. One technique is to use the backward wave oscillator approach. A small Russian company developed these sources with frequency operation up to 1.2 THz. The downside is the requirement of 2-10 KV to operate and the relatively bulky size. Some European and American efforts have sought to duplicate this technology, but have been unable to exceed 300 GHz. The RF approach that has received much more interest recently is the generation of low THz frequencies by multiplication. The surge of this activity was driven by the Herschel Space Observatory (European Space Agency), an observation satellite scheduled for launch in 2008. This platform will contain multiplier-based THz sources developed by Jet Propulsion Labs (JPL). An example of a JPL multiplier is shown in Figure 2.

Significant work is being done for THz signals that are generated by a lower frequency source and multiplied up to as high as a few THz [11, 39–41]. The heart of this signal generation is a Schottky diode used for the multiplication. This diode is housed in a metallic rectangular waveguide. The fabrication process for these small rectangular waveguides is receiving increased attention. Currently the use of metallic waveguides is the standard for signal propagation at these very high frequencies. The fabrication of these high frequency waveguides requires skilled technicians and expensive equipment. For applications where multiple units might be needed or for an array type of application, machining of several metallic waveguides can be very costly, if not prohibitive. A less expensive method to

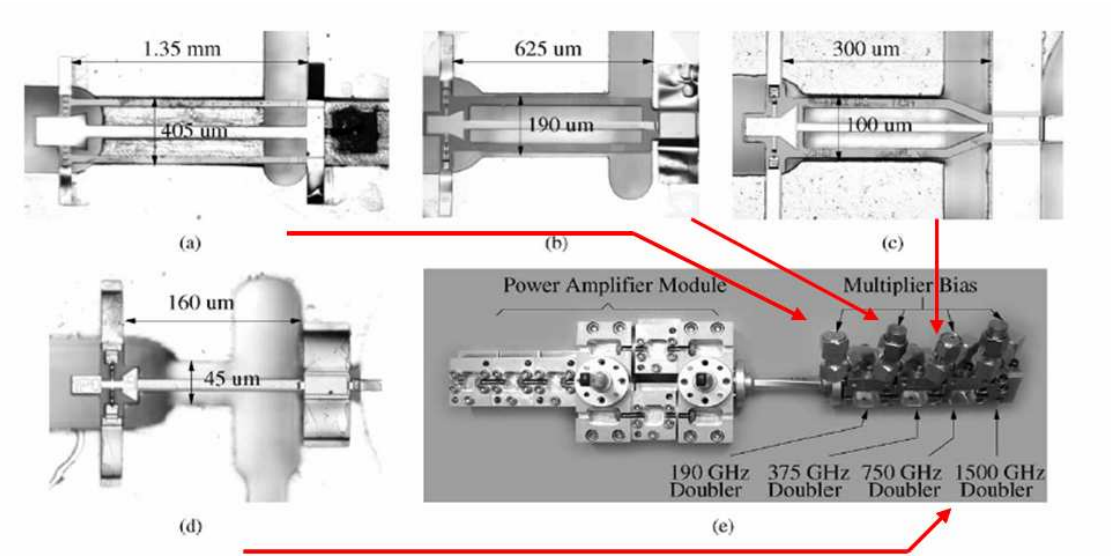

Figure 2: Example of a JPL multiplier module.

form these waveguides is needed, yet it must maintain the accuracy and performance of traditional waveguides.

There are alternative approaches in the research community being considered. The use of SU-8 has been demonstrated up to 320 GHz [14] although, the performance of the SU-8 formed waveguide compared to that of a traditional machined waveguide shows higher loss with increased frequency. Another approach used a hybrid style technique utilizing both silicon and SU-8 to form the waveguide components. This approach was demonstrated at 585 GHz [27]. However, the circuit was a mixer application, where the signal was coupled in via to an antenna rather than a direct connection. This did not allow for direct characterization of the waveguide in terms of loss. The third method is to use silicon micromachining to form the waveguides.

Etching of silicon to form waveguides is accomplished by one of three methods: wet etch, dry etch (Deep Reactive Ion Etch), and laser etching. Wet etching has been successfully implemented [9, 45] up to 250 GHz. Although the results have been very good, there are limitations to wet etching. A sloping profile with etch depth, as well as the inability to form stepped depths, limits the useful applications of this approach (e.g., the different size waveguides used in multipliers). Deep Reactive Ion Etching (DRIE) utilizing a Bosch Process can yield waveguide shapes with improvement over wet etching in terms of more

complex shapes and vertical side walls, but is also limited to a single etch depth. Arguably, the most promising approach is the use of a laser to etch the silicon into the desired shapes [60]. This technique excels as frequency increases (smaller waveguide dimensions) and has been shown to have excellent dimensional control and the ability to form complex shapes, such as a corrugated horn antennas [38]. This corrugated horn antenna pattern was measured at 2 THz. While this shows great promise for the use of laser etching silicon to form waveguides, little is known about the loss characteristics. This research will utilize the Deep RIE approach to form the silicon waveguides.

CHAPTER II

W-BAND OSCILLATOR

2.1 Introduction

Two W-Band oscillators, utilizing Raytheon's mHEMT substrate, are presented in this chapter. The various oscillator topologies are covered. A common source oscillator attempt is presented with the potential problems associated with its lack of functionality. Discrepancies are found between the model utilized and the measured data. A successful common gate oscillator, which functions at 96 GHz is presented . A unique method, using injection locking, is used to characterize the phase noise performance. Lastly, the successful common gate oscillator is compared to those available in the literature.

2.2 Oscillator Topologies

When considering the design of a W-band oscillator, the three basic choices for the active device topology are: common gate (base), common source (common emitter), and common drain (common collector). The common source is regarded as the configuration for high output power; the common gate is regarded as lower output power topology but does allow for easier tuning; and the common drain is regarded as a topology that is difficult to implement [20]. The initial topology was chosen as a common source. This allowed for relatively simple design and fabrication. However, it was discovered that a common gate approach yields a more unstable and controllable active device compared to the other two topologies. For the W-band oscillator designs, Raytheon's MHEMT process was used which has the following parameters: 100 um substrate thickness, 3 um of gold for metallization thickness, and a permittivity of 12.9.

2.3 Common Source Approach

The common source topology was the first configuration examined, because of the simplicity of its fabrication. When considering a common source approach, the feedback mechanism is placed in the source leads of the FET. A typical top view of a two-finger FET is shown in Figure 3. In this case the source leads are grounded through vias. To access these leads and insert the feedback mechanism, the vias are removed and placed further outside the FET.

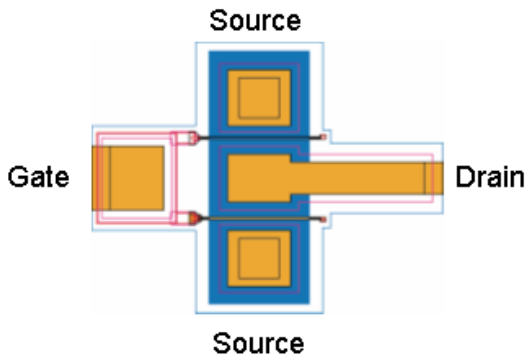

Figure 3: Top view of the FET layout.

The traditional negative resistance method was used for this design; a terminating network was placed on the gate lead, a feedback network on the source lead, and a matching network on the drain lead. A simple length of transmission line was used to increase the amount of source inductance and in turn increase the amount of feedback. An example of this is shown in Figure 4. The first design utilizing this approach produced very few functioning circuits. The problem of this approach was traced to discrepancies between the model and the end result of extending the source leads. A breakout the FET was measured and compared to the simulation in Figure 5. From Figure 5, it can be seen that the instability regions are in a different location and smaller Also the FET required operation at a much higher drain current level to even see a small amount of instability. Operating the FET at this high of a drain current level is not feasible as it is close to the damage level of the FET; most of the circuits were destroyed in the evaluation of this design due to the high current.

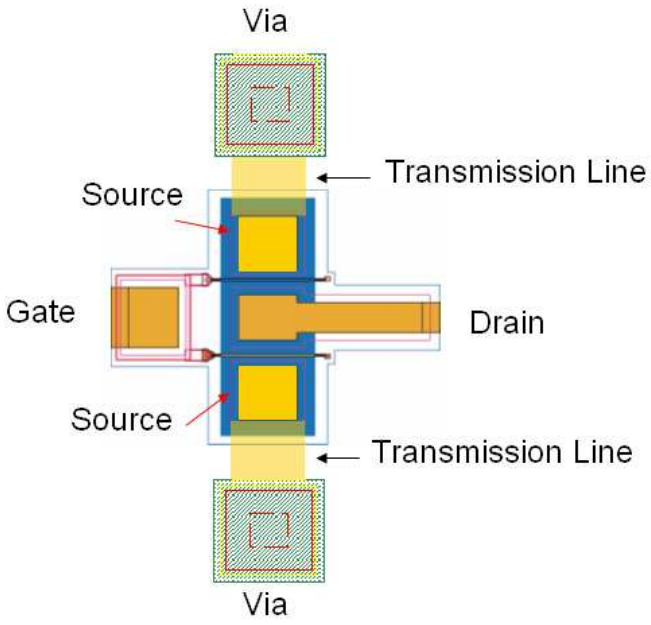

Figure 4: Top view of a FET layout with transmission lines in the source leads.

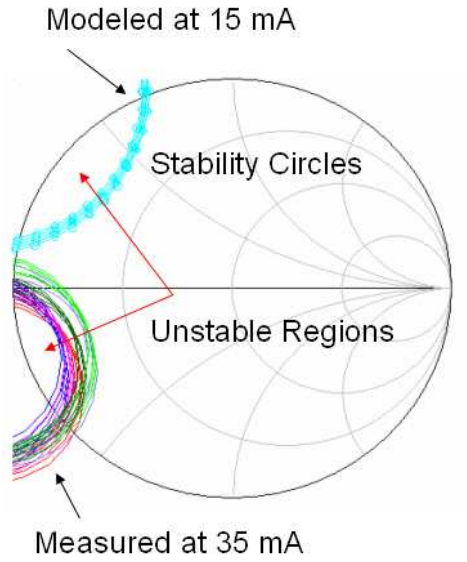

Figure 5: Plot of simulated and measured stability cirles for the common source design.

Rather than depart from this topology, an additional experiment was performed to ascertain if adding an additional length of transmission line (30 um and 50 um) to the first design would allow for sufficient instability when the FET is operated at the target current. The location of increase is shown in Figure 6. The measured results of this experiment are

shown in Figure 7. From Figure 7 it can be seen that even after adding the additional

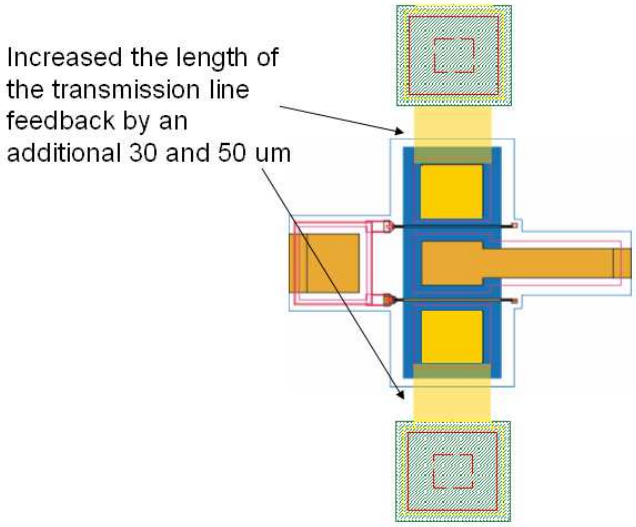

Figure 6: Top view of FET indicating where additional transmission length is placed in the source leads.

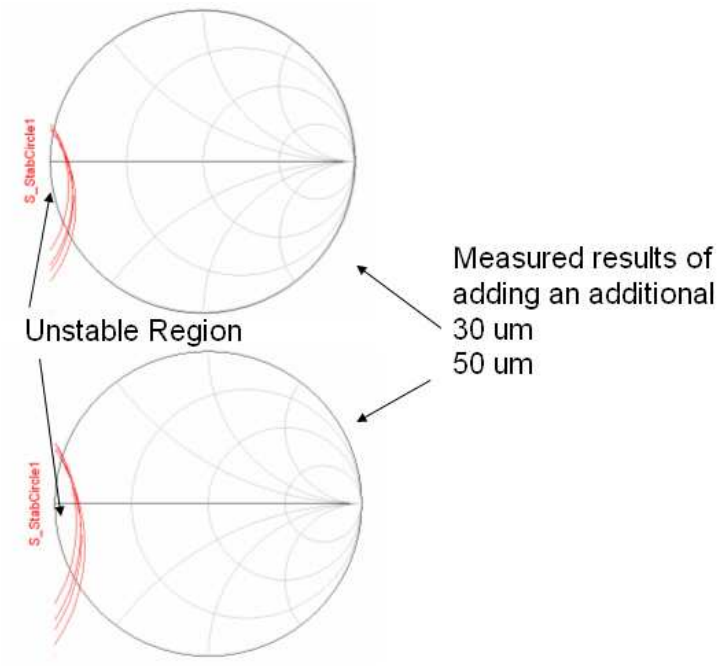

Figure 7: Measured results of the FET with additional transmission line lengths in the source leads.

amounts of transmission line to the source lead, the instability regions netted very small increases indicating that they are not suitable for an oscillator design when operating at

the lower drain current level. From these results it was decided to abandon the common source approach, and pursue a more promising topology.

2.4 Common Gate Design

From the previous section, it was determined that a more conservative choice of topology was required to accommodate a limited number of fabrication runs. After experimental simulation, and careful consideration to fabrication constraints, the common gate approach was elected.

While this is still a negative resistance design, it is approached in a slightly different manner than the traditional approach [21]. The first step in this approach is to select not only the FET parameters, but also the matching network (drain) and the feedback network (gate). All of these pieces of the oscillator act in a synergistic manner to set the range of possible oscillating frequencies. Although these networks operate together, the two passive networks serve specific functions within the oscillator circuit itslef. The gate network is the feedback path. Thus, the amount of feedback can be controlled by altering this network. The drain network primarily sets the negative impedance point, as well as provides the output matching of the circuit. Also of note is that both of these networks will be required to provide a path to apply DC bias to the FET. An ADS schematic view of the simulation is shown in Figure 8. From this schematic, the parameters of the FET, drain, and gate

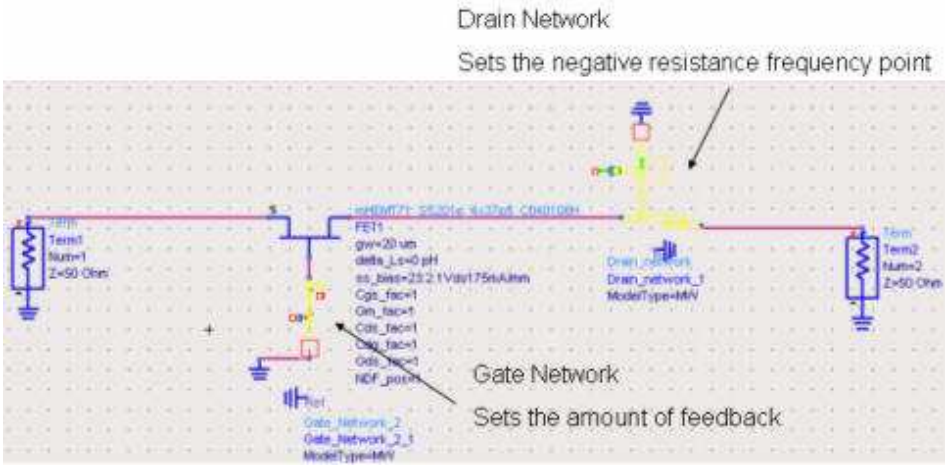

Figure 8: ADS schematic view of the FET, drain and gate networks.

networks are adjusted until the desired response is seen on the source port. The FET parameters used in the simulation were a 4X20 um FET with a bias point of Vd=2.1 and Id=175mA/mm or 14 mA. These networks are then simulated in ADS Momentum until the desired performance is achieved. A closer examination of the drain network is shown in Figure 9. From Figure 9 two distinctive elements can be observed; the bias leg and a coupled

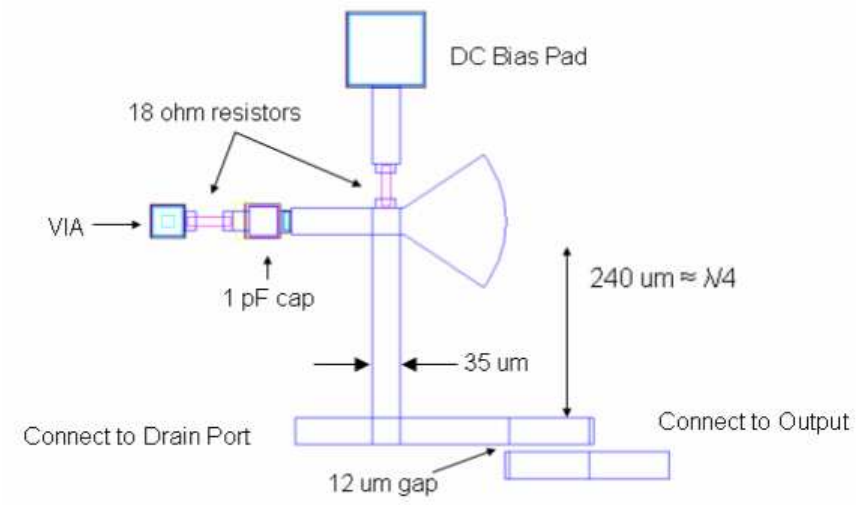

Figure 9: Layout of the drain network.

line section. It is desirable for the bias leg to look like an open circuit at the frequency of oscillation. This can be a difficult task when the bias line is loaded when a DC connection is made. Additional protection was implemented into the bias leg to deter the introduction of a feedback path at other frequencies through the DC bias source. For this, a short to ground through a capacitor is designed to short out as many frequencies as possible that might be introduced into the bias leg. The resistors were placed for added isolation in the path of the DC pad, and in between the via and the capacitor to help suppress any self-resonance. Finally, the output of the drain network was sent through a coupled line. This provides two useful functions; a filtering mechanism to null spurious signals, and more importantly the isolation of the circuit from DC bias. The latter was a very significant benefit, as it provided a much needed DC block in the event that the oscillator would be connected to another active device, such as an amplifier or mixer that has its own DC supply at that connection point.

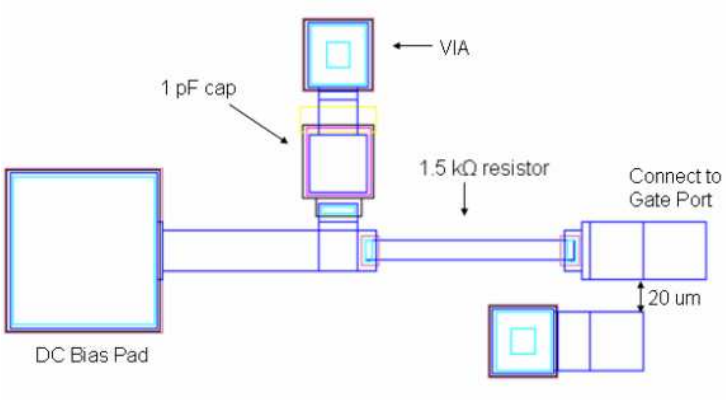

Figure 10: Layout of the gate network.

A more detailed view of the gate network is shown in Figure 10. During the design of the gate network, the desired amount of feedback was achieved at the desired frequency, but there was also feedback at other frequency ranges where oscillation was not desired. This led to using a small coupled line, which allowed the desired amount of coupling at the desired frequency, and reduced the amount of coupling at the undesired frequency ranges. The relatively high impedance value resistor provided a substantial amount of isolation to the DC bias pad and also attenuated any RF signal not handled by the coupling network. As another form of protection, a short to ground through a capacitor, is placed to handle any RF signal not sufficiently attenuated by the resistor as well as to provide an RF short to further isolate the DC bias pad. With these networks in place, the source port was examined (see Figure 8) to locate and tune the networks (gate and drain) until S11 was greater than 1 in the desired frequency range, and to insure that all other frequencies have an S11 less than 1. In this design the target frequency of oscillation is 95 GHz. The simulation results of the composite circuit are shown in Figure 11. From Figure 11 it is clear that the potential for oscillation is limited to the 95 GHz range as desired. It can be concluded here that the circuit is relatively safe with respect to not generating oscillations at undesired frequencies. A closer look at the frequency range of interest is shown in Figure 12. From Figure 12 it can be seen that the theoretical range where oscillations could occur is from approximately 92-99 GHz with the peak at 95 GHz. The target magnitude of S11 at 95 GHz was approximately 1.6. Although this may have been excessive in providing start-up power, it was decided

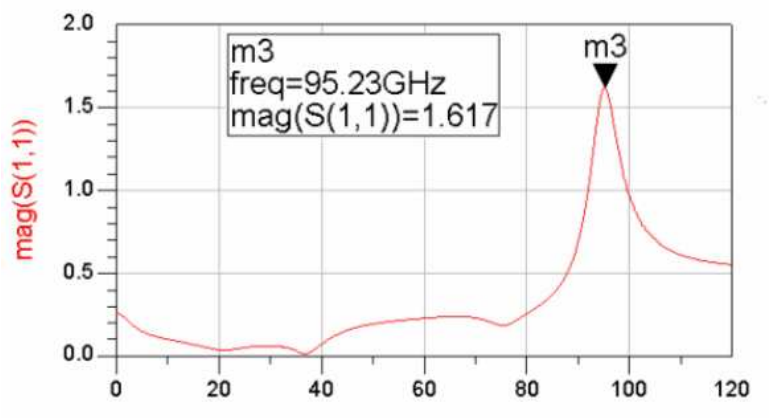

Figure 11: Simulation results looking in the source port of the FET with the gate and drain network attached.

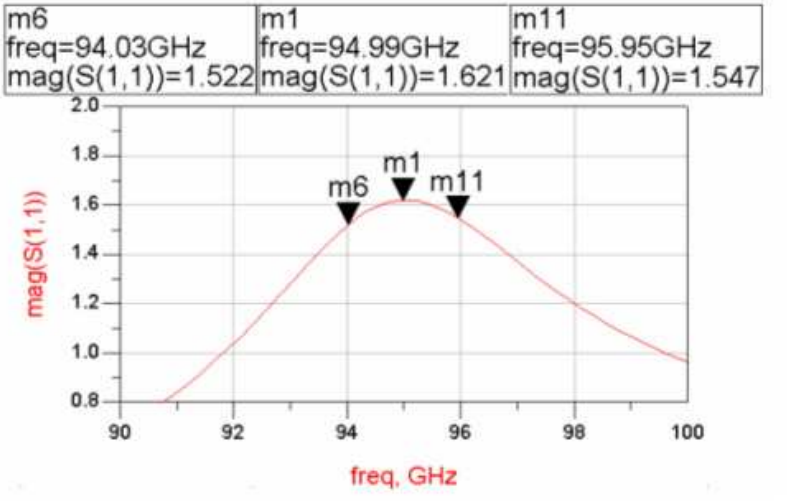

Figure 12: Simulation results over a smaller frequency range looking in the source port of the FET with the gate and drain network attached.

to err on the side of caution to ensure the highest possibility of a functioning circuit. The relationship of the magnitude of S11 to performance can be found in phase noise. A larger magnitude of S11 translates into an increased amount of phase noise; thus, it is ideal to keep this value as low as possible but still maintain a large enough value to have sufficient start-up power.

The remaining part of the circuit selection is the resonator, which will attach to the source port. To accomplish this, the reflection coefficient looking into the source is plotted in a Smith chart (see Figure 13). The reflection coefficients greater than 1 appear outside the unit circle of the Smith chart as expected . To facilitate the selection of the source

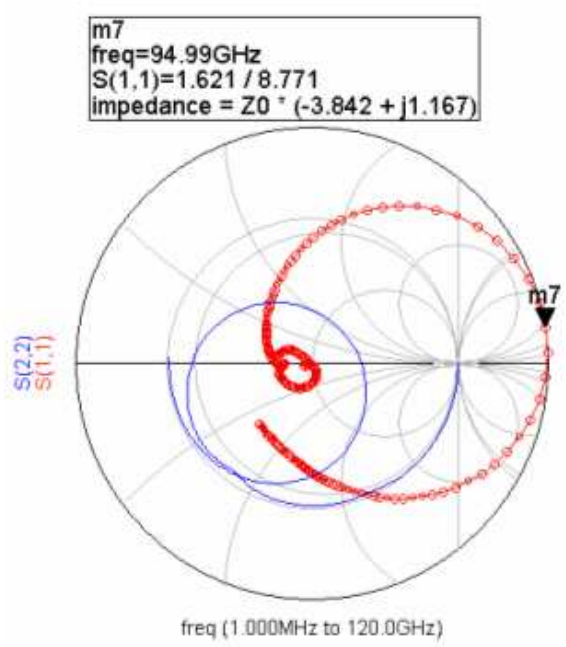

Figure 13: Smith chart plot of the simulation results looking in the source port of the FET with the gate and drain network attached.

network, the reflection coefficient looking into the source port of the FET is carried into the resonator plane by inverting the reflection coefficient. The resulting plot is shown in Figure 14, where the Smith chart plot is limited to just the unit circle. The resulting trace shown inside the unit circle is the portion of the reflection coefficient that is greater than 1, and the portion of the trace outside the Smith chart (not shown) has a reflection coefficient of less than 1. As the FET of the oscillator starts up and begins to move toward its steady state, the points on the trace inside the unit circle will begin to move toward the edge of the unit circle. From this, the impedance point of the resonator should lie near the marker of the desired frequency of oscillation.

When considering the layout for the resonator, one important point is that a DC path to ground exist for the grounding of the FET source lead. A resonator with a simple topology is desirable, so a simple tapped shorted stub resonator is chosen. A high-Q resonator is desired to achieve optimum phase noise. Another way to interpret a high-Q in terms of S-parameters is the steepness of the slope in the phase of the reflection coefficient of the resonator. The resulting resonator structure is shown in Figure 15 and the simulated response is shown

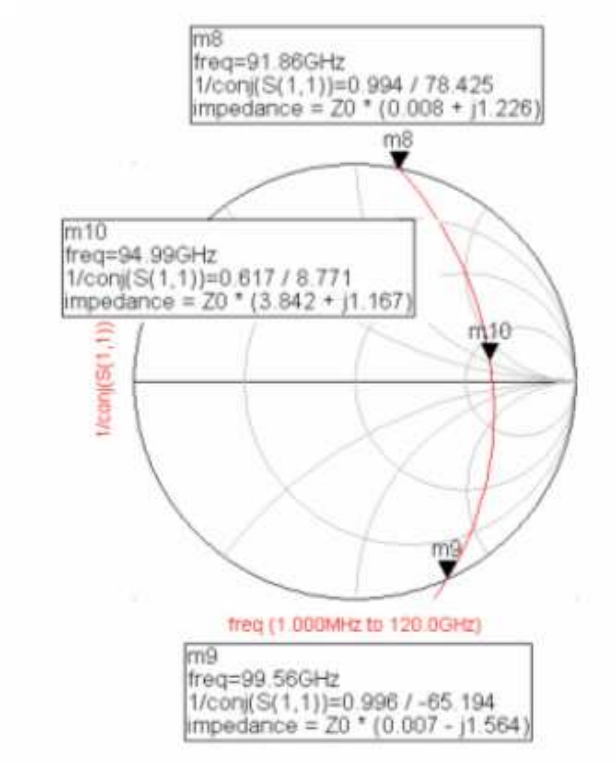

Figure 14: Simulation of the FET's reflection coefficient plotted in the resonator plane.

in Figure 16. The Smith chart in Figure 16 has both the resonator response (marker

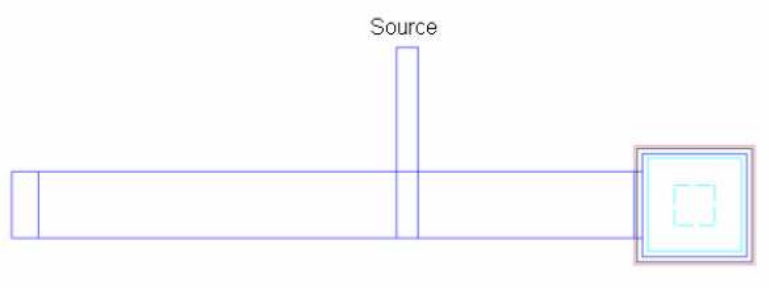

Figure 15: Resonator network layout.

m2) and the previously designed portion of the circuit (marker m1), which included the FET, drain network, and gate network. As previously mentioned, when the circuit starts up and begins to head toward saturation, the response will move toward the unit circle of the Smith chart (i.e., m1 will move toward the resonator trace). With the traditional way of approaching negative resistance design, the matching network is often made to be one-third of the negative impedance and the reactive part is made equal and opposite in

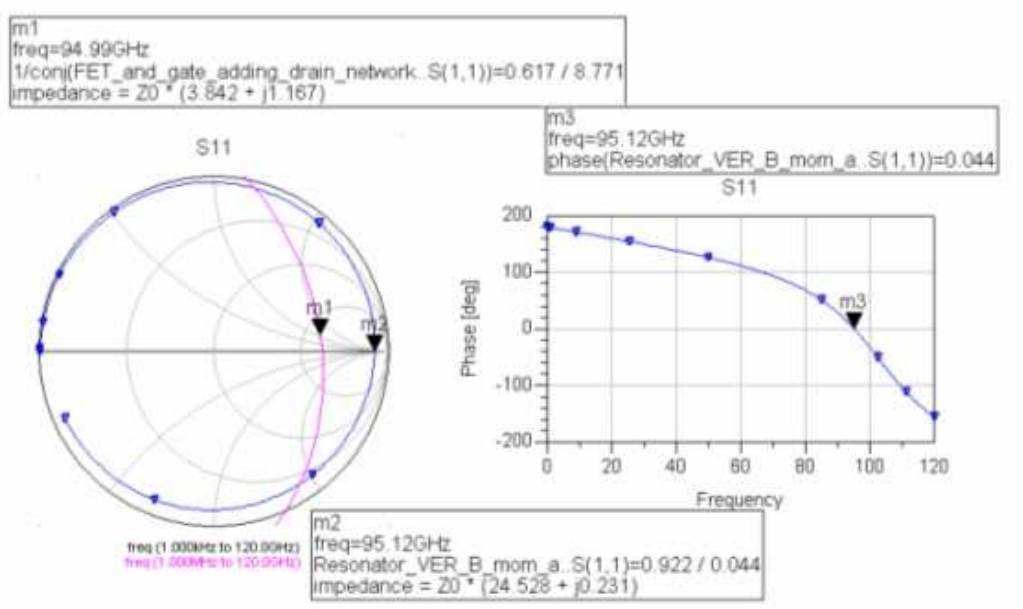

Figure 16: Simulation results of the resonator network (m2) along with the simulation results looking in to the source port of the FET with gate and drain network attached (m1).

value. However, this leaves some ambiguity in where the exact oscillation frequency will be, since the reactive impedance point will likely change in the FET and will be different from that impedance obtained when the FET is operated as an amplifier. There is similar ambiguity in the case of selecting the resonator impedance point as the 'path' of the FET response from startup to steady state, or when movement toward the unit circle is not exactly known. It is elected to set the frequency point of the resonator, 95 GHz, on the real impedance axis. This will correlate with a high slope response of the resonator and thus a high Q.

With the source network (resonator) selected, the circuit is complete. As a final step, the response of the circuit looking into the source port is examined for sensitivity to the FET processing. Specifically, two cases are examined: (1). -20% Cgs, -20% Gm, and + 20% Cds and (2). +20% Cgs, +20% Gm, and -20% Cds. The results of this analysis are shown in Figure 17. From Figure 17 it can be seen that these process variations could result in a shift up or down in frequency, in addition to some loss of amplitude. While the amplitude of the response or amount of feedback can be directly influenced by the DC bias applied, the

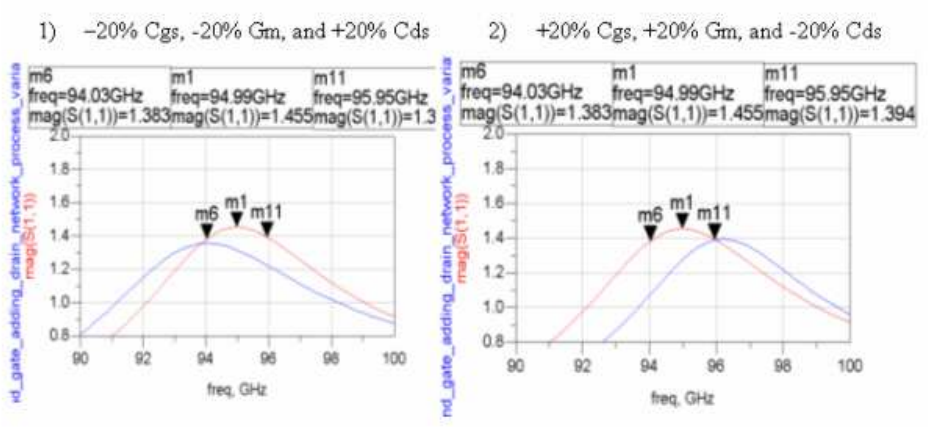

Figure 17: Sensitivity simulation results looking into the Source port of the FET with the gate and drain networks attached.

peak frequency point will only be minimally affected. To demonstrate this, different bias points were simulated using the nominal FET parameters. The results for three different bias points are shown in Figure 18; it can be seen that the amplitude increases with only a minimal shift in frequency. The completely assembled circuit is shown in Figure 19.

2.5 Common Gate Design Results

The chips are mounted with silver epoxy, and 10,000 pF off-chip capacitors are mounted as well after fabrication. The capacitors are then ribbon bonded to the DC bias pads on the gate and drain networks. This provides a needed RF path to ground that is not handled by the on-wafer capacitors because of their limited capacitance value. A picture of the fabricated circuit without the off-chip capacitors is shown in Figure 20. The oscillator was evaluated in three ways: unwanted oscillations, output power, and phase noise. As an initial step, the oscillator was checked for oscillations at frequencies other than the desired frequency. For a preliminary measurement, the oscillator's reflection coefficient was measured using an Agilent 8510XF Network Analyzer calibrated on-wafer using the multiline TRL calibration [44]. The WR-10 waveguide cutoff frequency of 59 GHz can be avoided since this setup uses Cascade Microtech 150 um Pitch 1mm coaxial probes. This allows for quick identification of frequency spans in which the reflection coefficient is greater than 0 dB, which can then be targeted for additional scrutiny. The measurement of the

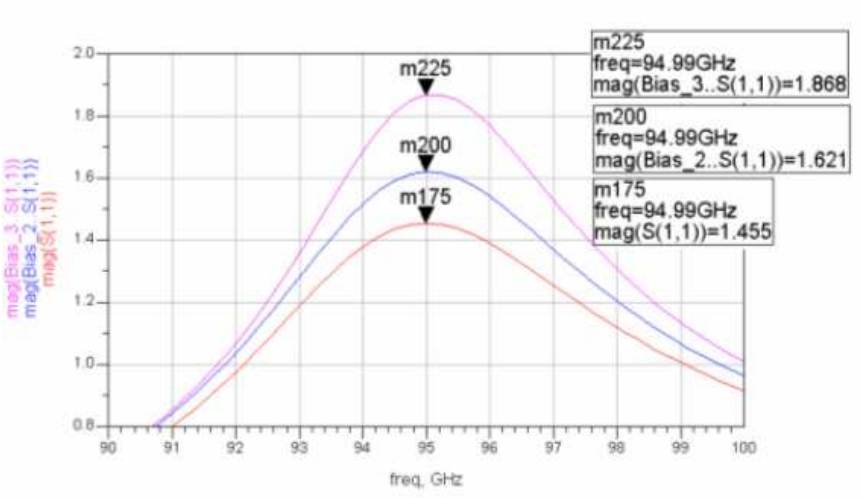

Figure 18: Simulation results looking into the source port of FET with the gate and drain networks attached for various drain current levels, 14mA, 16mA, and 18mA.

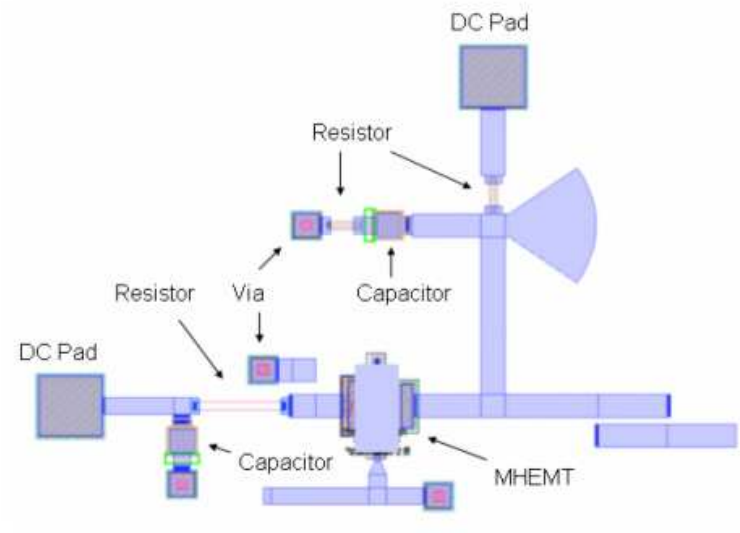

Figure 19: Layout of the complete oscillator circuit.

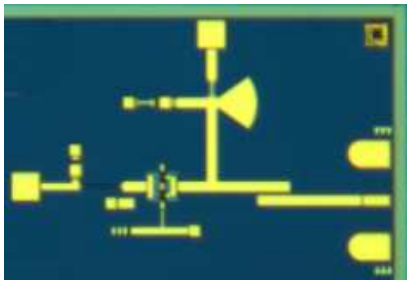

Figure 20: Photograph of the fabricated oscillator

reflection coefficient is shown in Figure 21 at various drain currents. From Figure 21, it can

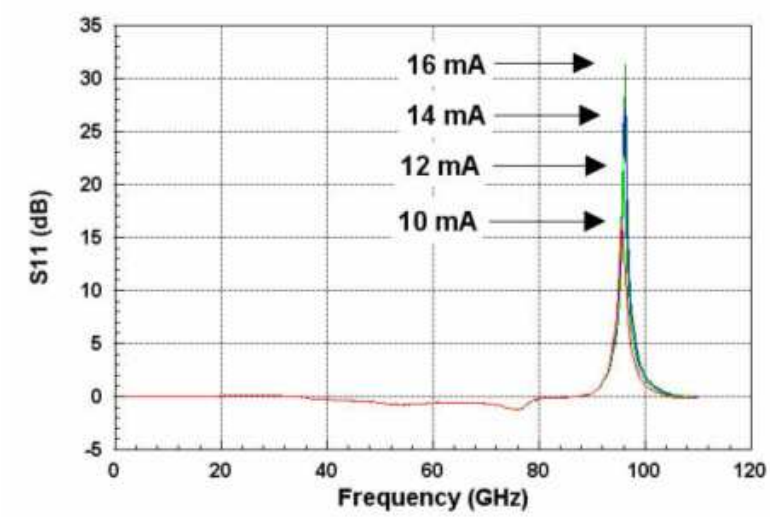

Figure 21: Reflection coefficient of the fabricated oscillator at various drain currents.

be observed that there are no other obvious oscillations at any frequencies other than those in the W-band frequency range (75-110 GHz). Hence, it is concluded that no additional scrutiny is needed to identify oscillations outside the W-band range.

For the power measurements, a Cascade ACP110-M WR-10 waveguide to 150 um pitch wafer probe was used along with a standard H-Plane waveguide bend. An Agilent W8486A W-band power sensor along with an Agilent E4419B power meter was used to detect the delivered power. The loss of the waveguide probe and the H-plane bend is conservatively estimated to be 1 dB and 0.1 dB, respectively, yielding a total loss of 1.1 dB, which will be added to the measured power. The measured maximum output power was +0.4 dBm, and the estimated output power was +1.5 dBm. Note that this power level was taken with a different bias condition than designed (2.5 Vdd and Id = 18 mA); this bias condition is also used for the phase noise evaluation for consistency and there was no significant degradation in the phase noise from the designed bias condition.

For the spectrum analysis, an Agilent 11970W W-band harmonic mixer was used in conjunction with an Agilent 8565E Spectrum Analyzer. The signal identification functions were utilized to identify a single W-band signal. The oscillator was injection locked with the Agilent 8510XF synthesized output signal to maintain the measurement accuracy

(i.e. no frequency drift from each measurement segment). In contrast with phase synchronization, such as with a phase-lock loop, small-signal injection locking provides frequency synchronization within a finite locking bandwidth realizable with a relatively simple hardware setup. When a free-running oscillator is injection locked, the instantaneous output frequency is equal to the injected signal. The phase noise of the locked oscillator at offset frequencies that lie within the locking bandwidth is suppressed [1, 71], and the phase noise beyond the locking bandwidth remains relatively unaffected. However, its free-running characteristics appear as phase variations that are a function of the unlocked phase noise, and are proportional to the locking bandwidth [25].

The oscillator is locked by hovering the 8510XF signal via a 1mm coaxial wafer probe near the gate network until the appropriate amount of power is coupled to achieve the lock. The frequency of the 8510XF is adjusted above and below the frequency of the chip oscillator to determine the locking bandwidth which was 500 kHz and used for later correction. The output spectrum of the oscillator at a 10 MHz bandwidth, shown in Figure 22, was corrected for the conversion loss of the harmonic mixer, which has a value of 37.5 dB at 96 GHz. It is

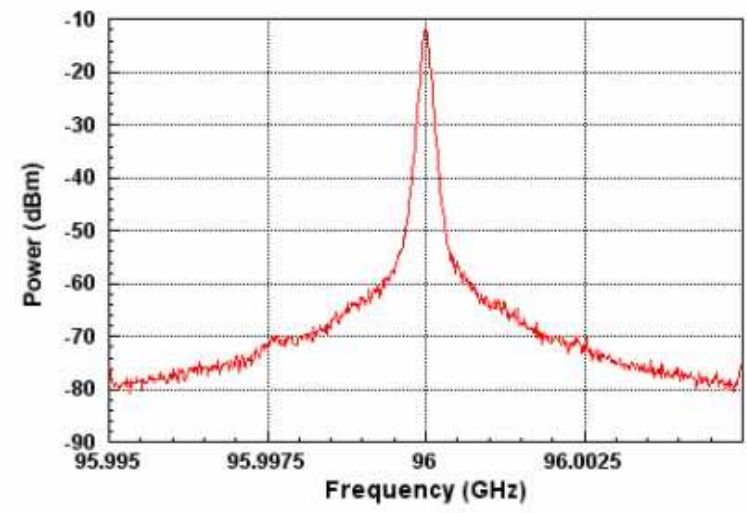

Figure 22: Spectrum output of the oscillator at 10 MHz span.

noted here that the specification for the noise floor of the harmonic mixer is -85 dBm at a resolution bandwidth of 1 kHz. During the measurements, the resolution bandwidth never exceeded 300 Hz, causing a small decrease in the noise floor. This small gain will likely not

exceed the losses of the wafer probe and H-Plane bend used in the measurement setup.

To achieve a high resolution for the phase noise measurements, it is necessary to break up the phase noise offset measurement into multiple segments. To correct the measurements for direct spectrum analyzer measurement, the following equation is utilized:

$$Ł'_{SSB} = P_{SSB}(f) - P_C - 10 * \log(NBW) + C \tag{2}$$

where $Ł'_{SSB}$ is the phase noise corrected to units of dBc/Hz, P_{SSB} is the measured power at each offset frequency point, P_C is the power of the signal at the center of oscillation, NBW is the noise bandwidth, and C is a log envelope correction factor, which is 2.51 dB [2]. The NBW is calculated from the resolution bandwidth by multiplying by a correction factor of 1.128 for a spectrum analyzer using a four-pole filter for the RBW filter [2]. The compilation of the multiple segments of data taken is shown in Figure 23. The data in

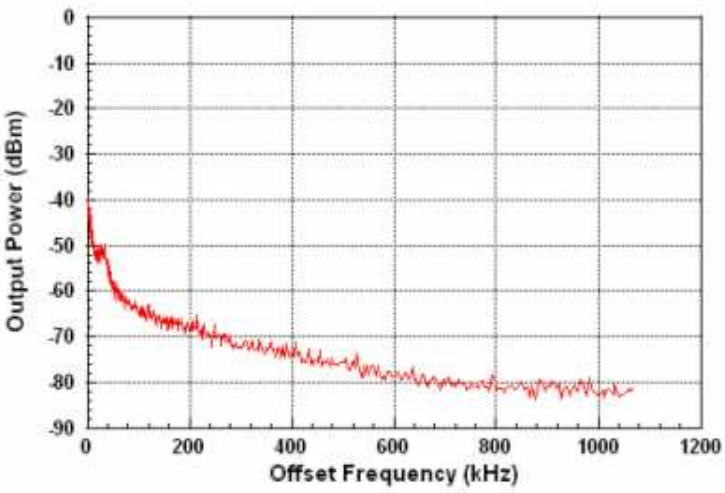

Figure 23: The uncorrected compilation of the spectrum output from the center frequency to an offset of 1 MHz.

Figure 23 is corrected for direct spectrum analyzer measurement, with the results shown in Figure 24. Figure 24 shows a highly distorted curve as a result of the suppression of the phase noise from the injection locking. To retrieve the actual phase noise of the oscillator from locked measurements, the locking effects must be characterized [2,25]. If the frequency of the injected signal is set equal to the nominal free-running frequency of the oscillator, knowledge of the locking bandwidth is sufficient to characterize the locking effects. In this

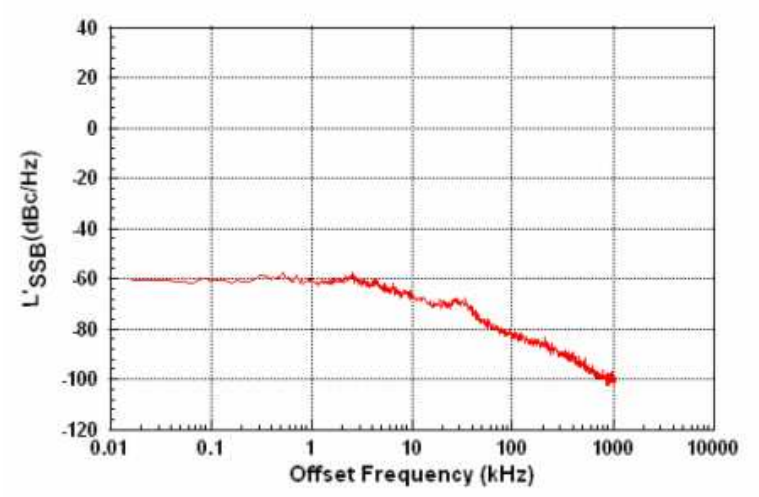

Figure 24: The spectrum output at an offset of 1 MHz corrected for direct spectrum analyzer measurement.

case, the free-running phase noise can be expressed in terms of the locked measured phase noise as [71]

$$Ł_{SSB} = L'_{SSB} + 10 * \log\left(\frac{f^2 + (0.5 * (B_{LOCK})^2}{f^2}\right) \tag{3}$$

where L_{SSB} is the single-sided phase noise measured with the spectrum analyzer, f is the offset frequency, and B_{LOCK} is the locking bandwidth. The oscillator phase noise corrected for injection locking shown in Figure 25 where it is understood that what is shown at close-in offset frequencies should be reported as $\frac{rad^2}{2}$/Hz.

However, it is customary to maintain the plot as the single-sideband phase noise, hence the greater than zero values. The oscillator exhibits an excellent phase noise response of -101 dBc/Hz at 1 MHz offset. The results are of particular interest, as this is the first W-band oscillator on an MHEMT substrate.

2.6 Comparison to State of the Art

An exhaustive publication search concluded that this work is the first W-Band oscillator on an mHEMT substrate. With this in mind, this work will be compared to oscillators on other types of substrates. The other works were on pHEMT substrates, InP substrates, SiGe substrates and some other exotic substrates.

Generally when comparing oscillators at this frequency, the key performance factors

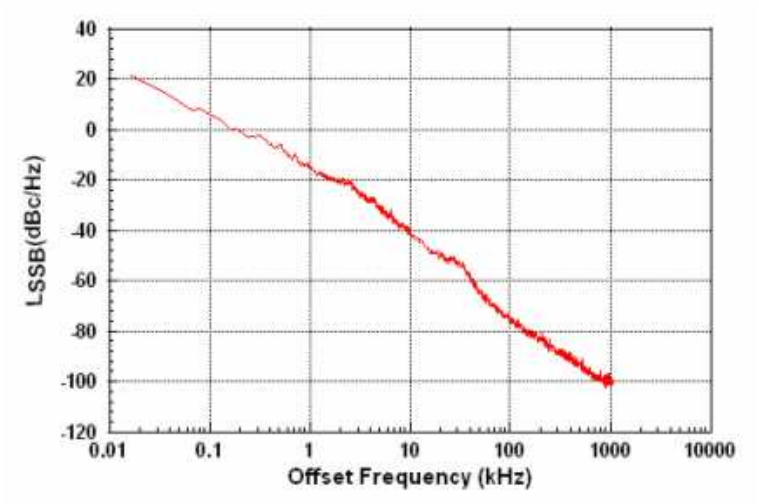

Figure 25: The fully corrected phase noise output of the oscillator up to 1 MHz offset.

to examine are the phase noise and output power. An examination of multiple types of oscillators is shown in Figure 26. In this figure the Y-axis contains the phase noise of each oscillator at a 1 MHz offset and the X-axis indicates each oscillators operating frequency. Also included in the plot is the output power of each oscillator in parentheses, the indication of 'amp' if the output power was amplified, and 'multiply' is this was a lower frequency oscillator that was multiplied to attain a W-band signal.

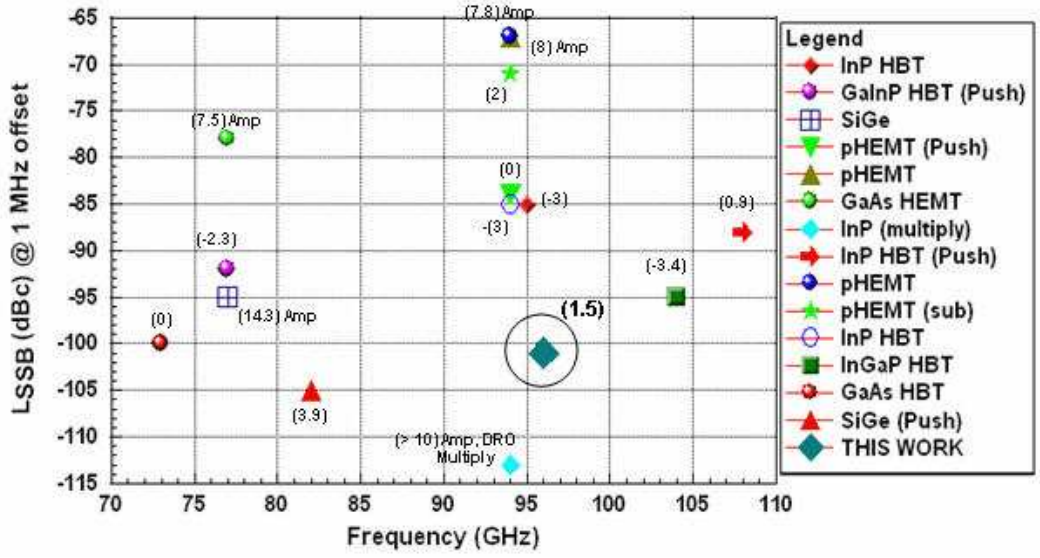

Figure 26: Comparison of W-Band Oscillators

An additional method of comparison is to use a figure of merit that attempts to encompass key factors of the oscillator. This can make a comparison of various oscillators much more efficient. A popular figures of merit is [26]:

$$FOM = L(f_{offset}) + 10 * log(P_{DC}) - 20 * log(\frac{f_{osc}}{f_{offset}}) \quad (4)$$

where $L(f_{offset})$ is the phase noise at some offset frequency (typically 1 MHz), P_{DC} is the DC power consumption of the oscillator in mW, and f_{osc} is the frequency of oscillation. This figure of merit is applied to the oscillators with sufficient data included in the literature (see Figure 26) and is summarized in Table 2. From this table, it can be seen that the oscillator from this work is among the state of the art published in the available literature.

Table 2: A comparison of recently published W-Band oscillators using the previously defined figure of merit.

Ref	$Pout(dBm)$	L(dBc/Hz)	$P_{DC}(mW)$	$Freq(GHz)$	FOM
[64]	3.5	-105	280	82	-179
[31]	0.92	-88	204	108	-165.6
[7]	-5	-85	78	94	-165.5
[58]	-3.4	-95	32.4	104	-180.2
[65]	3.5	-105	140	75	-181
[3]	-9	-80	24	80	-164.3
[55]	7.5	-75	130	78	-151.7
[18]	-7.5	-97.5	25	85	-182.1
[37]	18.5	-97	2600	77	-160.6
[52]	-6	-87	60	85	-169.0
[10]	-14	-87	15.5	90	-174.2
$This\ Work$	1.5	-101	45	96	-184

2.7 Summary

In this chapter, two W-Band oscillator were presented. A common source oscillator attempt was presented along with the potential problems associated with its lack of functionality. The discrepancies between the utilized model and data were highlighted. A successful common gate oscillator utilizing an mHEMT substrate at W-band was presented, functioning

at 96 GHz, with an output power of 1.5 dBm. A unique method of injection locking was utilized to characterize the phase noise performance of -101 dBc/Hz at 1 MHz offset. The performance of this oscillator was compared to the state of the art available in literature and found to have excellent performance.

CHAPTER III

SILICON WAVEGUIDE

3.1 Introduction

In this chapter, silicon micromachined waveguide is proposed as a replacement to traditional metallic machined waveguide. A thorough analysis of the approach used for the silicon waveguide is presented. Measurement considerations are analyzed and addressed. The contents of this chapter demonstrate the feasibility of the use of silicon waveguide as a replacement for traditional machined waveguide, and for the first time silicon micromachined waveguide is characterized at 400 GHz.

3.2 Fabrication Consideration

When considering the split of the waveguide there are two basic options: (1) cut the block in the E-plane or (2) cut the block in the H-plane as shown in Figure 27 [48]. The traditional

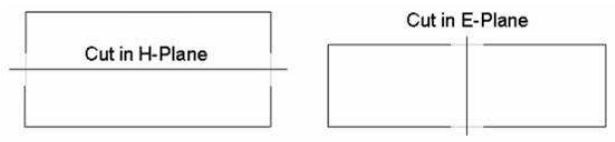

Figure 27: Illustration of the two options for splitting the waveguide block.

split-block style waveguide is generally cut in the E-Plane to avoid the potential for non-canceling higher-order modes at the junction of the split. An examination of the potential problems associated with both splits was carried out via simulation using Ansofts's HFSS with a waveguide size of WR-2.5 (635 X 317.5 um). During the analysis, a case with a gap in the E-plane and a case with a gap in the H-plane were varied in both length and width. The length and width of the gap were varied symmetrically on both sides of the waveguide. An example of the setup is shown in Figure 28. The S-parameter results for a gap width of 5 um for each case are shown in Figure 29 and Figure 30.

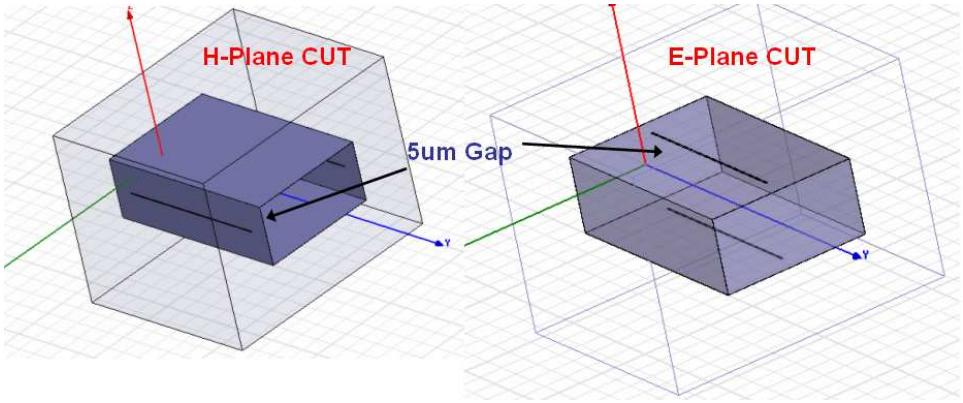

Figure 28: HFSS setup for analysis of E-Plane and H-plane splitting.

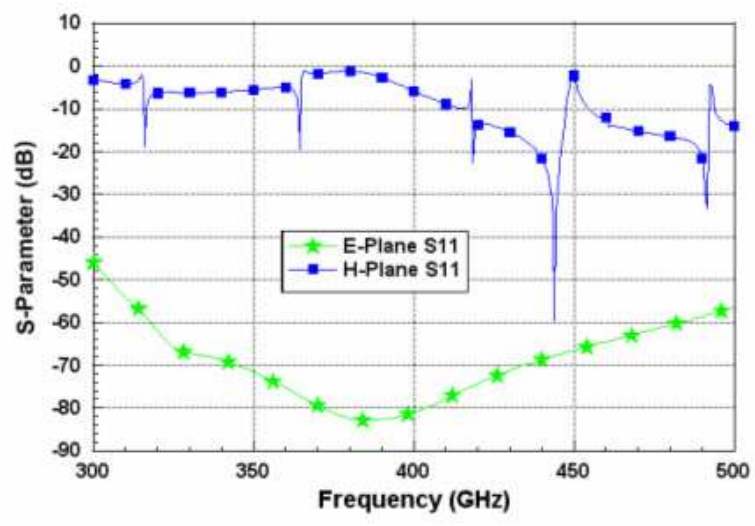

Figure 29: Reflection coefficient of the simulation of the both the E-plane and H-plane gap of 5 um.

The case with the gap in the H-plane showed significantly greater sensitivity when the gap size was small, while the E-plane gap was very resilient to a relatively large gap. A further examination of the two cases, focusing specifically on the fields is shown in Figure 31 and Figure 32. From these results, it can be clearly seen that there is a significant amount of leakage in the case of an H-plane cut. This size and symmetry of a gap may not occur in practice; however, it demonstrates the extreme difference between the two cases and the E-plane cut is more desirable.

The waveguide size is WR-2.5, with dimensions of 25 X 12.5 mils (635 X 317.5 um). The waveguide is fabricated in a split-block fashion using two identical pieces. The examination

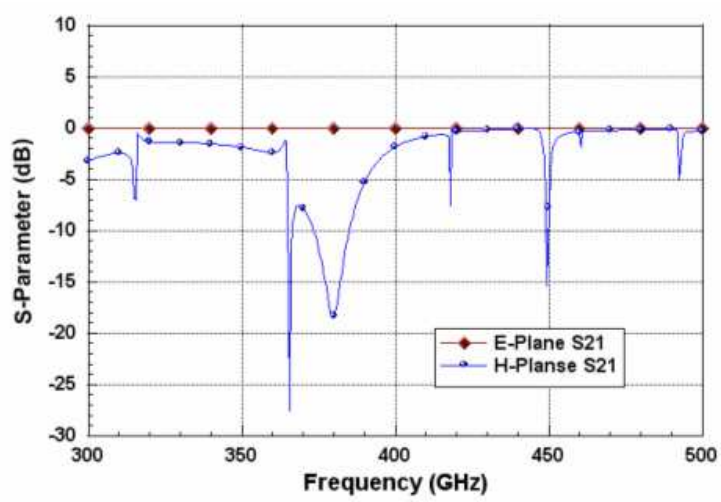

Figure 30: Transmission coefficient of the simulation of the both the E-plane and H-plane gap of 5 um.

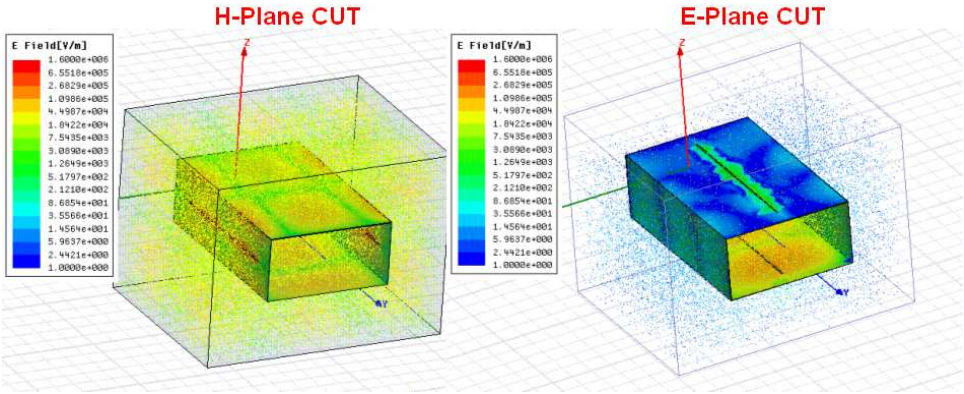

Figure 31: The E-Field plot of the both the E-plane and H-plane gap of 5 um.

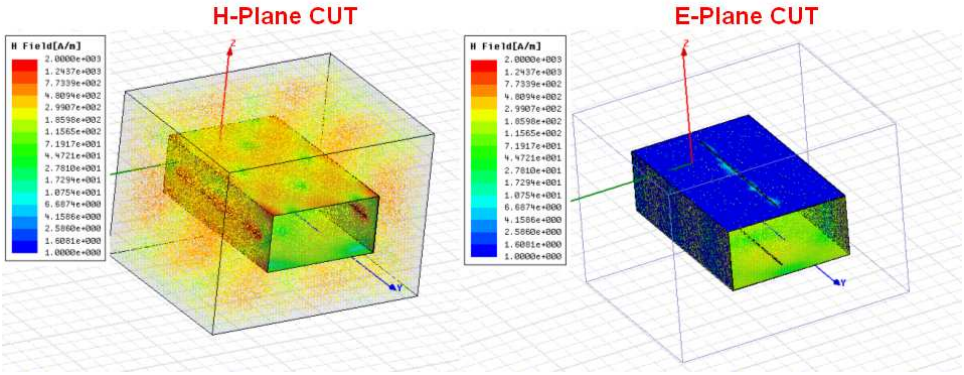

Figure 32: The H-Field plot of the both the E-plane and H-plane gap of 5 um.

of the two splitting options demonstrated that an E-plane cut approach would be more ideal. The H-plane was selected since it allowed for a smaller etch depth (∼160 um) in comparison to the E-plane (∼320 um) cut when considering the same waveguide size. The structural integrity of the etched wafers was a concern since 400 um thick wafers were used.

3.3 Fabrication Procedure

High-resistivity silicon wafers ($\rho > 5$ kohm-cm), with a thickness of 400 um, were used in the fabrication. After a standard cleaning of the wafer, AZ-P4620 or SPR-220 photoresist was spun onto the wafer to a thickness of approximately 8 um. This photoresist was then exposed by using a UV light through a properly defined mask. The patterned is defined by using AZ400K developer for AZ-4620 photoresist or Shipley's 319 developer for SPR-220 photoresist. The patterned wafer is then mounted to another wafer of the same size using Cool Grease to protect the backside for future processing.

The etching process is performed using a Deep Reactive Ion etching system (DRIE). Specifically, a Bosch process is used to allow for a more vertical etch [67]. Although the Bosch process allows for near vertical etching, there is still a taper associated with the etch. This can be problematic, particularly with relatively deep etching. A best-case and worst-case result is shown in Figure 33.The left picture shows a good result with very little

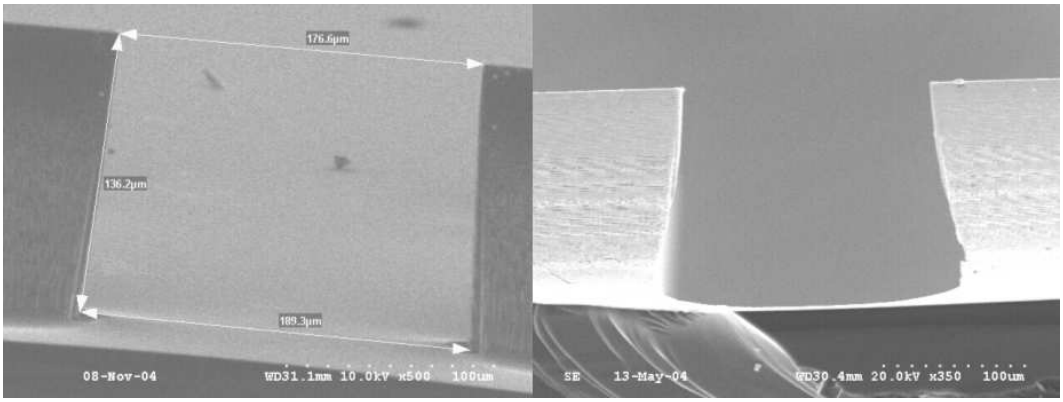

Figure 33: Examples of the vertical nature of the Bosch process for a good case (left) and poor case (right).

taper, while the right picture shows a significant amount of taper, where the thickness of the wall was too narrow and actually etched through.

After the initial etching, or top side etching, the wafer is thoroughly cleaned to remove all photoresist. The wafer is then flipped over and the back side is defined in a similar manner to the top side. The alignment of the etched front side with the pattern on the back side is a critical step; care must be taken to assure that the individual silicon pieces will be released with near planar edges from top side to back side. After the alignment, exposure, and developing, the wafer is mounted to another wafer and the etch is completed. Upon completion of the etch, each of the silicon pieces are removed and cleaned as thoroughly as possible using acetone, isopropyl alcohol and, if necessary, piranha etch (sulfuric acid and hydrogen peroxide). A graphical summary of the steps are shown in Figure 34. Successfully fabricated pieces are shown in Figure 35, displaying the sample at the end of the topside process and at the end of the entire etch process.

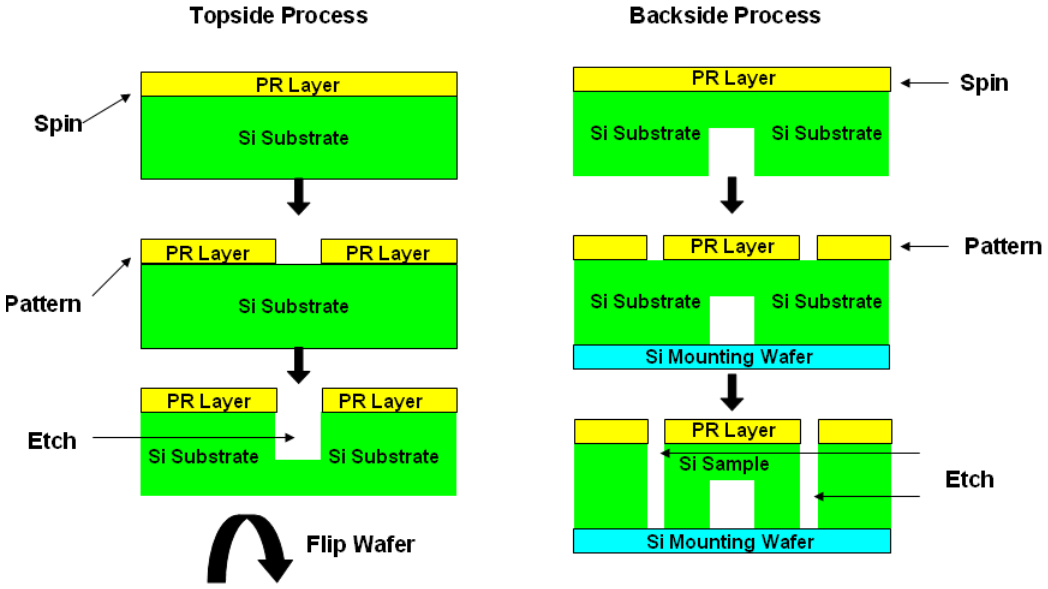

Figure 34: The fabrication steps utilized in forming the silicon straight waveguide.

The final step in the fabrication is metallization. The method used was a sputtering technique that included titanium as an adhesion layer followed by copper and gold. This method was chosen due to its isotropic deposition, which is necessary to cover the relatively deep silicon trenches. The total metal thickness deposited in the waveguide trench was initially 2 um, that was later increased to a total of 5 um. Each piece was metallized on both sides to prevent leakage into the silicon.

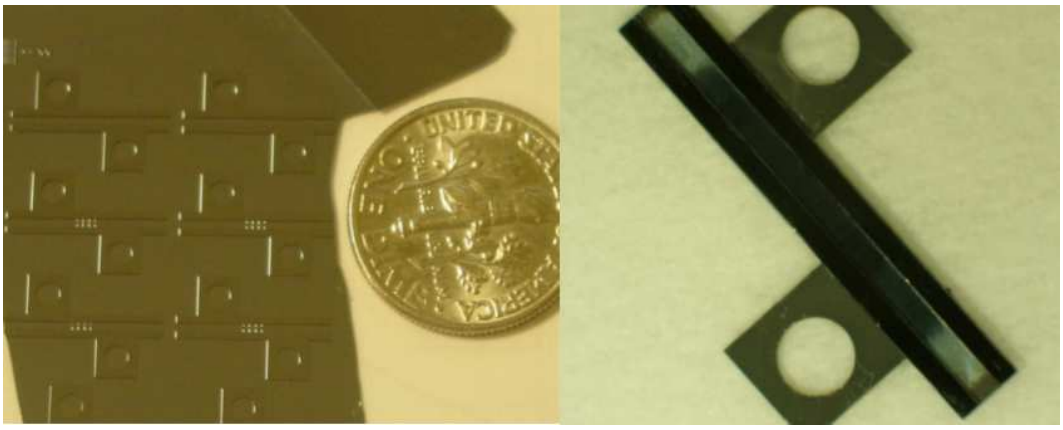

Figure 35: Examples of the fabrication after the top side processing (left) and after the fabrication is complete (right).

3.4 Measurement Fixture

In order to test and characterize the silicon waveguide, it must be interfaced with measurement equipment. A standardized MIL F3922/67B flange pattern is used when dealing with rectangular waveguide of this size, whose patter is shown in Figure 36. Since it is not possible to machine this pattern into the silicon pieces, a fixture must be used for the interfacing of the silicon to measurement equipment. This fixture will also provide a way to bring the two pieces together to form the rectangular shape and avoid the need for any type of bonding.

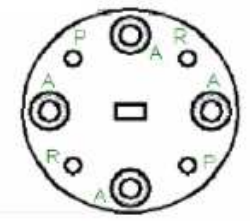

Figure 36: Examples of a standard flange pattern. A is the threaded screw hole, P is where an alignment pin is inserted and R is the receptacle for the pin on the mating piece.

The fixture was designed to fit precisely around each piece of the silicon waveguide. Openings already designed and fabricated into the silicon pieces allowed for screws to secure the silicon pieces into each half of the fixture. One half of the fixture has alignment pins, the other half has receptacle holes for those corresponding pins. When brought together, the

two halves should be well aligned. Before construction of the fixture, additional analysis was performed to analyze the electrical effects of the fixture. The entire fixture was constructed in Ansoft's HFSS and is shown Figure 37. The size of the entire fixture, relative to the

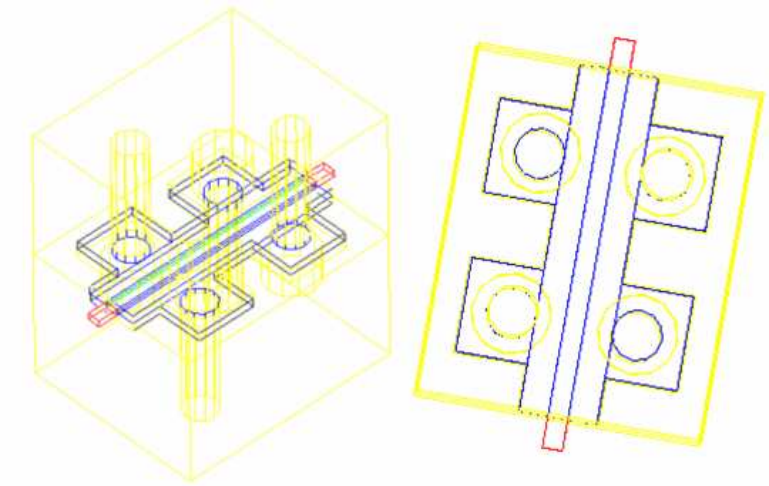

Figure 37: Layout for fixture in Ansoft's HFSS.

wavelength, was extreme and made the simulation unsolvable. A reduction of the model, as well as the use of symmetry planes, was done to make the simulation more manageable with the result shown in Figure 38.

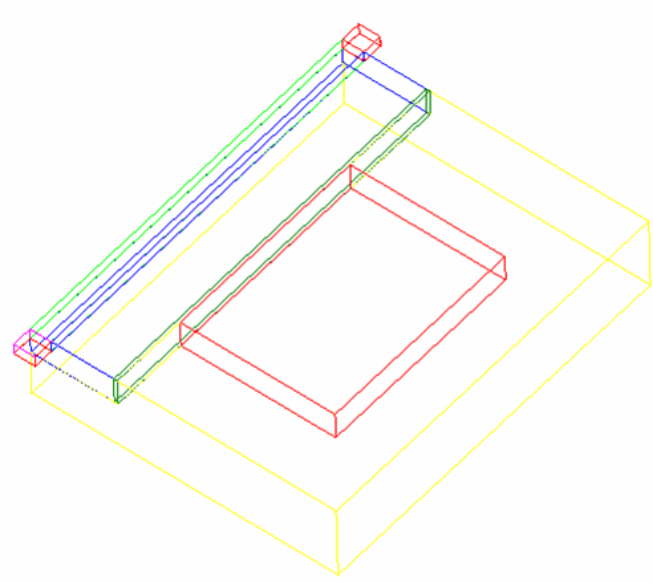

Figure 38: Reduced layout of the fixture in Ansoft's HFSS.

First, an ideal case was performed, where the test ports of the simulation were sized

exactly to those of the silicon waveguide. Only the waveguide trench was assigned as a metal material and the rest of the waveguide was assigned as silicon. The fixture was assigned as brass. The results of this ideal simulation are shown in Figure 39 where it can be seen that the E-field is confined completely in the waveguide. Because of both the small

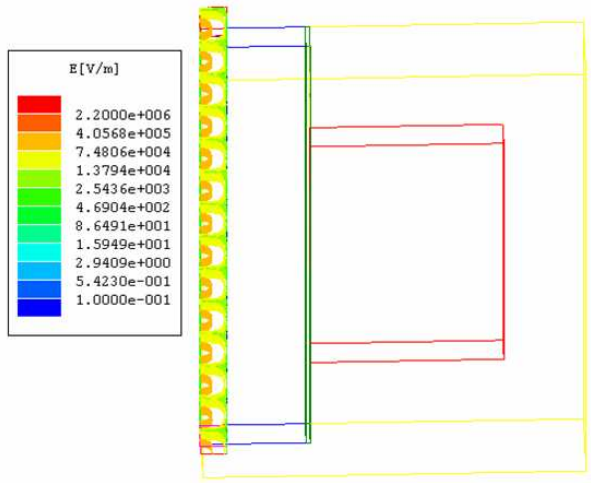

Figure 39: Simulation of ideal case with only the waveguide trench containing metal. The E-field is shown.

dimensions of the waveguide and the consideration of the taper that the silicon piece will have, a mismatch of the test port to the silicon port is a very real possibility. To examine the potential effect of this mismatch, the same simulation was run with an exaggerated test port size. The results of this simulation are shown in Figure 40, where as significant amount of leakage is seen propagating into both the silicon piece and the cavity of the fixture. In a normal metal-to-metal measurement setup this leakage would not occur. The signal easily propagates through the silicon and into the fixture cavity since the exposed silicon is only semi-insulating. This problem can be easily remedied, by metallizing the mating face of the silicon, resulting in a metal to metal contact. The same simulation was run again adding a metallized surface to the mating face of the silicon. The results are shown in Figure 41. This demonstrates the need, not only for metallizing the trench of the waveguide, but, also the mating face of the silicon waveguide. Both sides of the silicon piece were metallized which left no exposed silicon surface To help eliminate this potential problem.

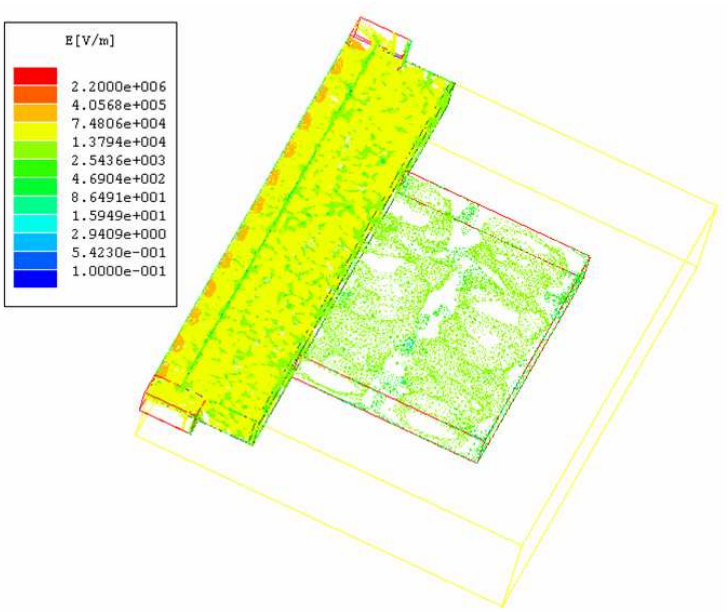

Figure 40: Simulation where the test port mating to the waveguide is enlarged to see the leakage effects. The E-field is shown.

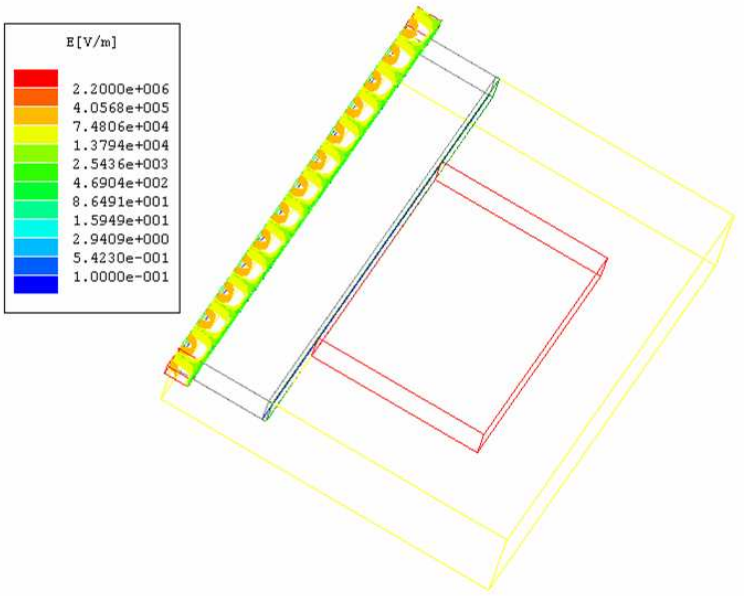

Figure 41: Simulation of the fixture with a larger test port than the waveguide port, the face of the waveguide is now metallized. The E-field is shown.

3.5 Measurements

When performing measurements at frequencies above 110 GHz, the availability of sufficient efficient equipment is limited. For measurement up to 325 GHz, Olsen Microwave Labs

manufactures frequency extension modules that interface with Anritsu and Agilent network analyzers [19]. Olsen has also manufactured some prototype frequency extension modules up to 500 GHz; however, the dynamic range of the modules is limited to less than 30 dB. A second alternative would be to use a signal generator at lower frequencies (< 100 GHz) and multiply up to the desired frequency. Virginia Diodes specializes in multipliers up to 1.7 THz [16]. Lastly, there is the AB Millimetre Network Analyzer, with capabilities up to 1 THz [49], that has a dynamic range of 60 dB at 400 GHz.

A strong relationship with Jet Propulsion Laboratory (JPL) in Pasadena, California allowed for the use of the AB Millimetre Network Analyzer System. The analyzer output was outfitted with waveguide transitions to allow an interface of a WR-2.5 waveguide size to match the silicon waveguide.

As covered in the previous section, in order to interface with the metallic waveguide of the measurement setup, a fixture was fabricated out of brass to hold the silicon pieces together. The fixture provides a good seal between the two halves of silicon, as well as providing proper alignment between the silicon pieces and the metallic measurement interface. For the fixture-to-measurement interface alignment, a standard MIL F3922/67B flange was patterned on the fixture using slightly tighter tolerances to ensure good alignment. A photo of the holder both assembled and with only one half is shown in Figure 42. A close-up picture of the silicon waveguide opening when the pieces are in the holder is shown in Figure 43.

Figure 42: Photograph on the metal waveguide holder for the silicon pieces.

To have a fair comparison to the silicon waveguide, a brass waveguide in the same shape

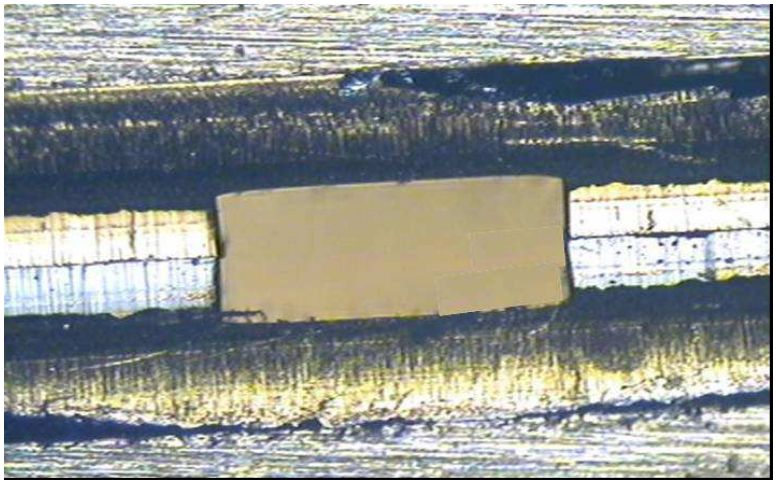

Figure 43: A close up view of the waveguide opening of the silicon pieces.

and dimensions as the silicon waveguide was fabricated. The metal waveguide fit into the same fixture as the silicon waveguide.

The AB Millimetre Network Analyzer is an excellent tool for measurements ranging from 100 GHz to well over 1 THz and provided an excellent amount of frequency and dynamic range within one unit of equipment. The AB system is shown in Figure 44 and Figure 45. A drawback of the system is the potential for the introduction of noise to the data. There is no traditional calibration method available for this analyzer, nor is this measurement NIST traceable. Each frequency point is set up one at a time and the system is 'zeroed out' by taking a base measurement with no DUT present. The DUT is then inserted and the sweep is taken. For these measurements, the analyzer was capable of sweeping 2 GHz, 1 GHz below the center frequency and 1 GHz above. It is common for the analyzer to swing +/- 2 dB around the center frequency because of the standing waves inherent to the system. The data is curve fitted using a third order polynomial to draw a good conclusion. For an example of the curve fit versus measured data, the metal waveguide insert was measured and fitted, and is shown in Figure 46.

Figure 46 shows that a third order polynomial fits reasonably well and shows a good representation of the data in a clear and concise so conclusions can be made. Figure 47 shows the measurement again of the metallic waveguide along with the silicon waveguide. The two waveguides show very good agreement, with the silicon piece showing slightly more

Figure 44: The rack of supporting equipment for the AB network analyzer.

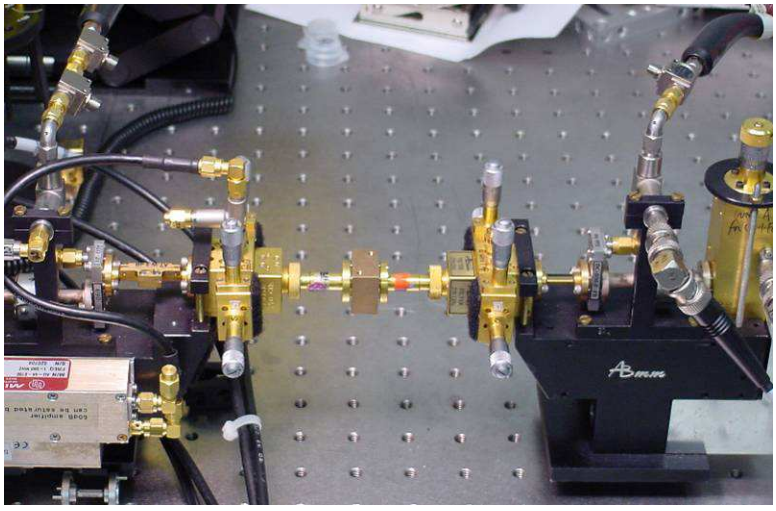

Figure 45: The measurement heads of the AB network analyzer with the metal holder (DUT) shown in the middle

loss than the metallic piece. The average loss of the metal insert is approximately 0.51 dB and the average loss of the silicon waveguide is approximately 1.02 dB for 11.8 mm of length.

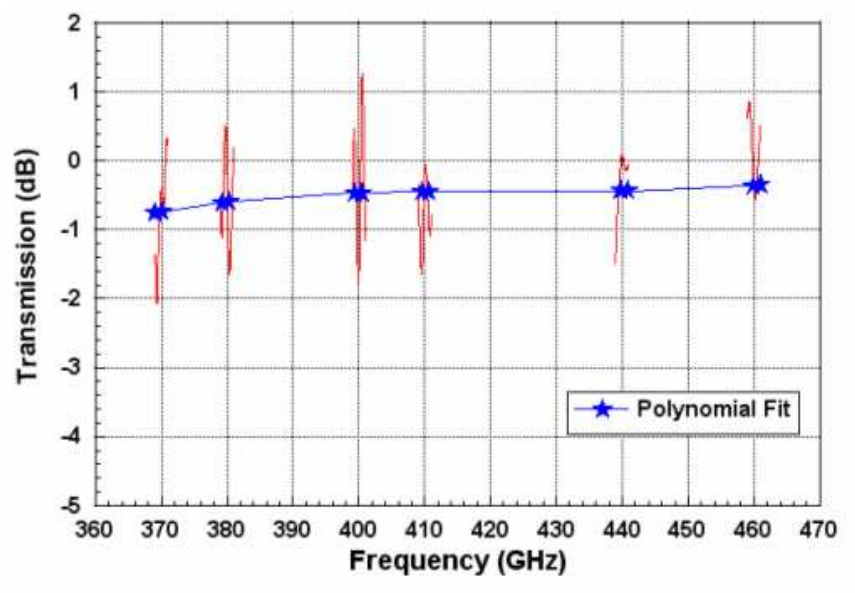

Figure 46: Measurement versus curve fit of the metal waveguide inserts.

For comparison, a theoretical loss is calculated and plotted in Figure 47, using the following equation:

$$\alpha = \frac{\lambda}{b\lambda_g}\left(\frac{\pi}{\lambda\eta\sigma}\right)^{\frac{1}{2}}\left[1+\left(\frac{\lambda_g}{\lambda_c}\right)^2\left(1+2\frac{b}{a}\right)\right]8.676\frac{dB}{m} \tag{5}$$

where a and b are waveguide dimensions, λ_g is the guided wavelength, λ is the free space wavelength, λ_c is the cutoff wavelength, η is the impedance of free space, σ is the conductivity of gold $(4.1 * 10^7 S/m)$. In addition, the result of the calculation is multiplied by 1.3 to account for surface roughness effects [17]. The larger loss of the silicon waveguide could be attributed to a few possible causes. The slight slope of the silicon waveguide causes an improper interface with the measurement system and creates small gaps for energy to leak out. This is something not present on the metal insert (see Figure 48 for an example). The split in the H-plane could also cause some additional losses as well as the condition of the surfaces. An optical profilometer analysis was performed on the broad surface of the metal and silicon waveguides. It was determined that the surfaces are comparable, but the silicon guide actually had a more uniform flat surface.

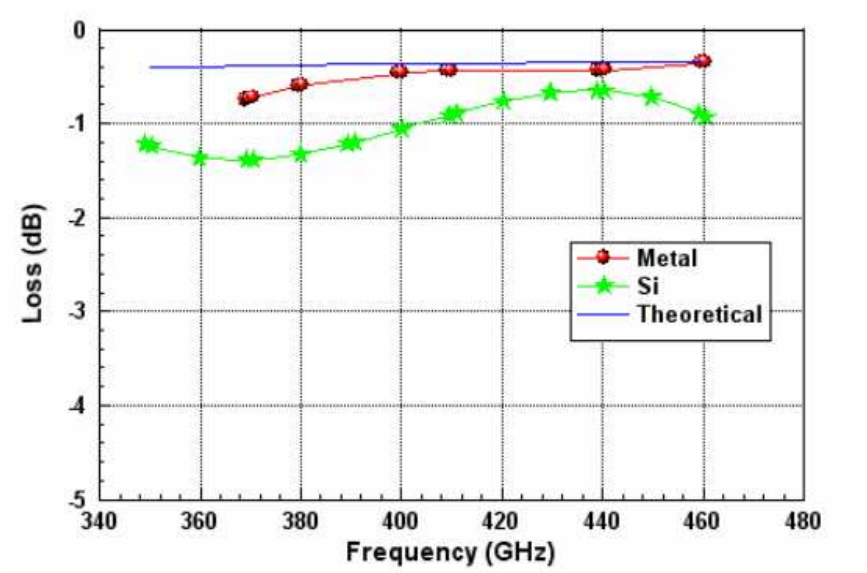

Figure 47: Measurement of the Silicon waveguide, the metal waveguide insert and a theoretical loss.

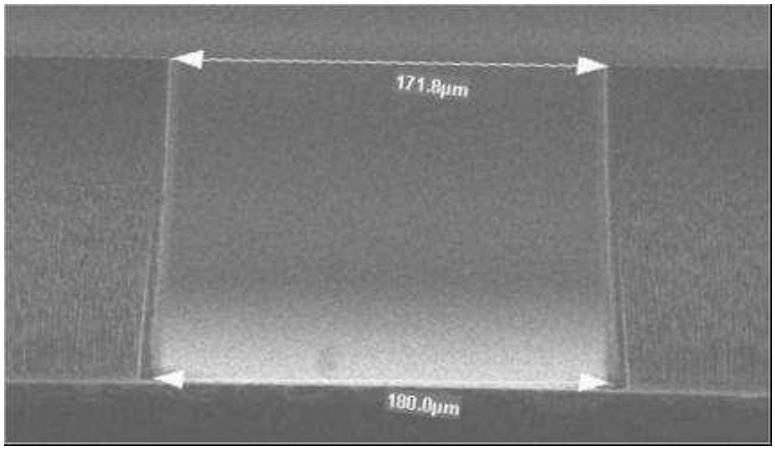

Figure 48: SEM showing the slope associated with the DRIE etch.

3.6 Summary

In this chapter, a thorough examination of the design, fabrication and measurement of silicon waveguide was covered. To date, this is the first ever silicon waveguide characterized at 400 GHz. This accomplishment demonstrates the feasibility of using silicon waveguide in place of traditional metallic waveguide. The presented ground work addressed the fabrication using a Deep RIE etch, the packaging and assembly of the silicon waveguide, and the difficulties associated with the measurement.

CHAPTER IV

SILICON MULTIPLIER

4.1 Introduction

In this chapter a silicon micromachined waveguide multiplier, using an HBV diode, will be examined. A brief review of diodes utilized in multiplier applications above 100 GHz will be given. The HBV diode will be introduced and the benefits of using an HBV diode will be delineated. The method of creating the silicon micromachined rectangular waveguide multiplier block will be covered. An extensive review of the measurement setup, necessary to characterize a multiplier of this type, will be given. A through description of the fixture utilized for the measurement will be presented. The second of two different measurements demonstrated excellent performance. This measurement showed very little difference between the metal waveguide block and the silicon micromachined block.

4.2 HBV Diode

For any type of multiplier, a nonlinear component is necessary. This component allows for the generation of the harmonics of the fundamental signal. The primary leader for devices when considering multiplication beyond 100 GHz is Schottky varactor diodes [11,16,39–42]. Schottky diodes have been utilized for multipliers at frequencies of 100 GHz up to 2.7 THz and are a proven technology for this application. Applications utilizing Schottky diodes generally require a bias network, which must be considered in the design process. This can add an extra layer of complication in some cases. A frequency doubler is utilized for relatively lower frequency operation and high power output, . To extend performance to higher frequencies, a tripler application is utilized. These designs are generally more difficult since they require an idler circuit to feedback the second harmonic to be multiplied up to the third harmonic.

An alternative to using the proven Schottky diode is the heterostructure barrier varactor

(HBV) diode. The HBV diode is a relatively new active device and was only introduced in 1989 [32]. The HBV diode is a unipolar device that has a symmetric capacitance-voltage characteristic which will only generate odd harmonics (3rd, 5th, etc). This is a very valuable characteristic as it negates the need for idler circuits for a tripler application. Also this type of diode requires no bias and removes the need for any bias circuity. The design in this chapter will utilize an HBV diode, fabricated by the University of Virginia.

4.3 Fabrication

The design for this multiplier was fabricated in metal waveguide block by the University of Virginia [69]. The basic design of the multiplier is shown in Figure 49. The design of the

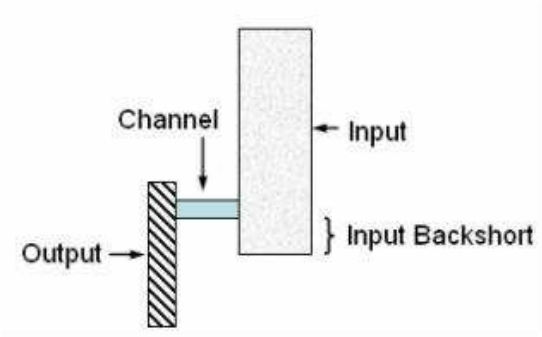

Figure 49: Basic layout of the multiplier block.

multiplier block can be summarized into the following three basic sections: input, channel, and output. The input section of the block is WR-10 (2.54 mm X 1.27 mm). This section is the input of the multiplier with the critical feature being the backshort length. The channel of the multiplier is where the diode chip is seated. The output section of the multiplier is WR-3 (0.864 X 0.432 mm) waveguide size. If the multiplier were to fabricated in equal halves split in the E-plane, the etch depths required would be 1.27 mm, 0.177 or 0.056 mm, and 0.432 mm respectively. This might be possible using a laser etch technique [60], but it is not possible using the chosen DRIE technique. With this in mind, a stacked approach must be utilized to create the necessary waveguide sizes as depicted in Figure 50. Each half of the block will be formed by three silicon pieces utilizing two different wafer thicknesses. The method of fabrication is similar to that of the silicon micromachined straight waveguide

(see section 3.3). The finished pieces are also metalized with titanium, gold, and copper to a thickness of approximately 5 um.

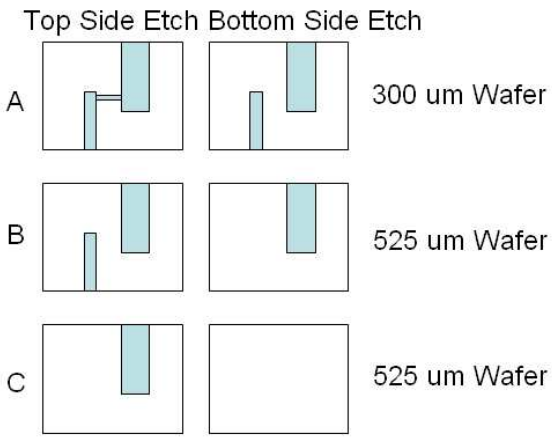

Figure 50: The etch steps utilized for the three layers of silicon that form one-half of the multiplier block.

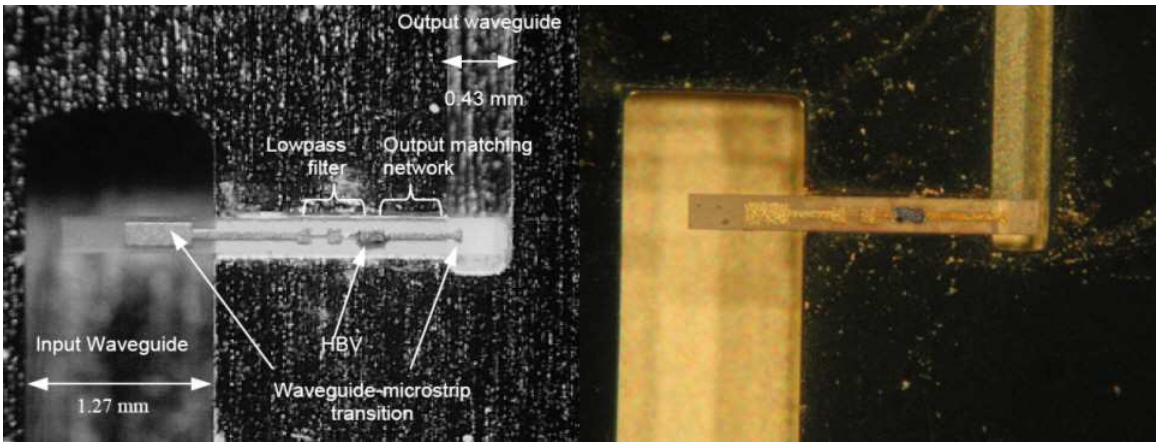

Figure 51: A comparison of the metal block and the silicon micromachined block with the diode chip mounted in the channel.

A comparison of the metal block and the silicon block, focused on the portion where the diode chip is mounted, is shown in Figure 51. Figure 52 shows the stack-up of the silicon after placing the next layer over the diode (totalling four layers).

4.4 Measurement Setup

Sufficient power must be generated to test the multiplier since high frequency multipliers have relatively low conversion loss. The desired delivered power for this setup is 100 mW

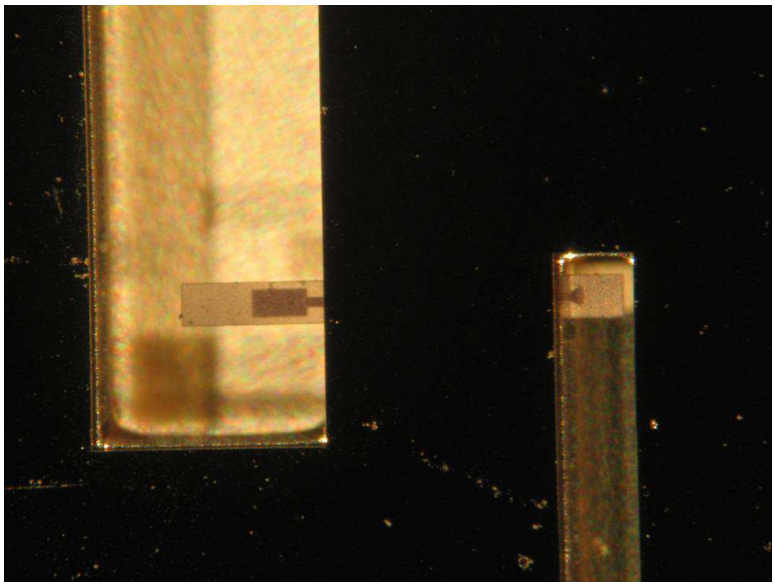

Figure 52: The silicon multiplier block with the next layer inserted. A total of four of the six silicon layers are shown.

(20 dBm). The input frequency range for the multiplier is 87 to 93 GHz. Althought network analyzers (Anritsu, Agilent) have the ability to generate such frequencies, their output power levels at these frequencies are limited to +8 to -10 dBm (6 to 0.1 mW) which is well below the necessary power level. Consequently, the traditional frequency synthesizer approach is not appropriate for this type of measurement.

Another more appropriate option for this type of measurement is the use of multipliers. A multiplier chain allows for much higher generation of power as compared to a synthesizer setup. The down side of using a multiplier setup is the bandwidth ($\sim$10%). The measurement was performed at the University of Virginia in conjunction with Virginia Diodes, Inc. The basic setup of the measurement system is shown in Figure 53. The frequency is initiated in the setup by an Agilent E8247C Signal Generator. This signal generator provides a signal from 10.875 to 11.625 GHz. This signal is fed into a Spacek Labs amplifier to provide a high drive level for the Spacek quadrupler. The frequency at this point is in the range of 43.5 to 46.5 GHz. The output of the quadrupler is WR-19 waveguide. This output is fed through a WR-19 waveguide variable attenuator. This attenuator will help control the drive level, if necessary, to the next multiplier. The final multiplier is a D-90 doubler from Virginia Diodes, Inc. The input is WR-19 and the output is WR-10. This doubler provides

an output of >100 mW from 87 to 93 GHz. An isolator is attached to the output of this doubler to maintain a good match. This output is fed into a WR-10 variable attenuator. This will allow a method to control the amount on input power to the DUT. The next piece in the base setup is a WR-10 directional coupler. The coupler is setup is configured to measure the reflected power from the DUT. This power is measured via a diode detector and is connected to the coupled-port of the coupler by a variable attenuator. The amount of reflection is displayed as a voltage on a DMM. The last two pieces of the setup are power senors and meters.

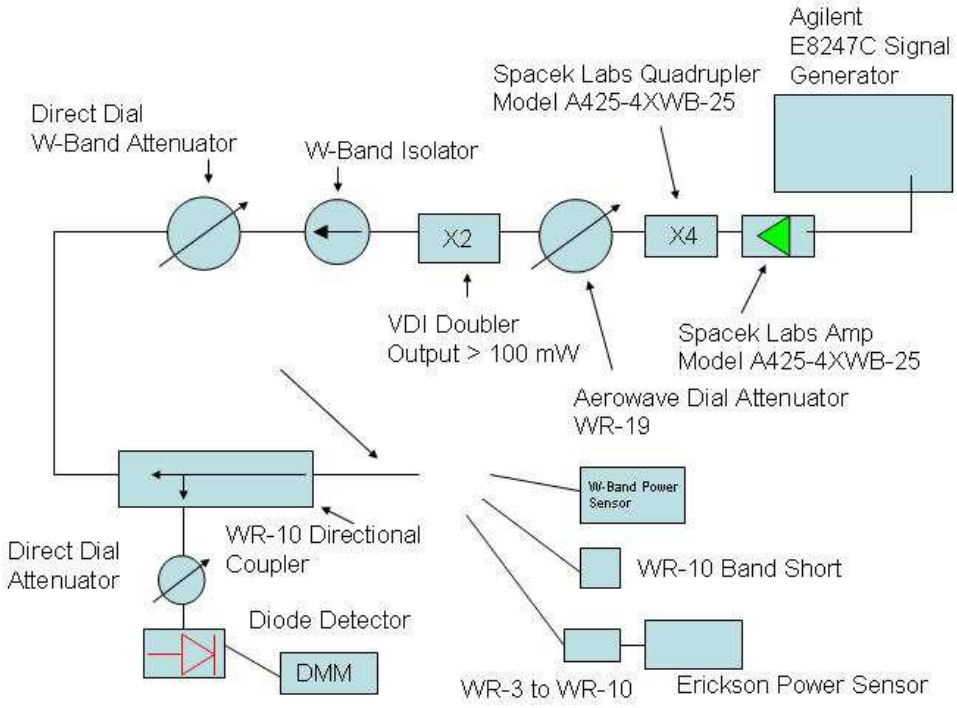

Figure 53: Block diagram of the measurement setup to characterize the multiplier.

The power level delivered to the DUT must be known to calibrate the system. An Agilent W-Band power sensor is utilized to characterize the power level at the end of the WR-10 coupler. The power level can then be adjusted using the WR-10 variable attenuator. The reflection voltages must also be calibrated. This is accomplished by placing a waveguide short on the output of the coupler. Since the output power of the coupler has been determined and can be varied by the WR-10 attenuator, the voltage read for the diode detector can be interpreted as a complete reflection of the DUT, in this case a waveguide

short. It should be noted that this must be done at every frequency point.

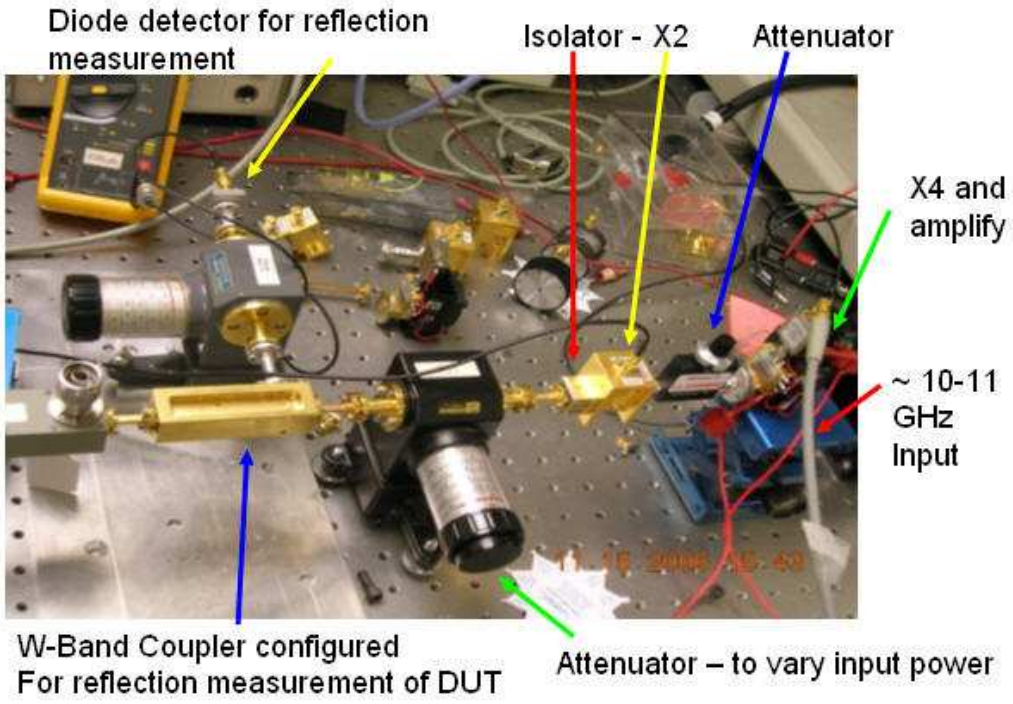

Figure 54: A photograph of the measurement setup used to characterize the multiplier.

Finally, since the DUT in this case is a multiplier (tripler), the output will be beyond the range of most power meter and sensors. The output power is measured by an Erickson PM2 power meter and sensor which has power measurement capabilities into the low THz frequency range. The output of the multiplier is WR-3 and the input to the Erickson power sensor is WR-10. A WR-3 to WR-10 transition is therefore utilized to minimize reflections.

4.5 Measurement Fixture

As with the silicon micromachined straight waveguide, a measurement fixture will be required to characterize the silicon micromachined based multiplier. Since the multiplier block is composed of six layers of silicon wafers, the fixture must be able to hold the stack up in place with sufficient alignment. Rather than try to form the fixture around the silicon pieces, as was done with the straight waveguide, the silicon pieces are integrated more precisely with the fixture. Using Autodesk©, the measurement fixture was constructed with the silicon layers. This process allowed for a more precise alignment between the silicon

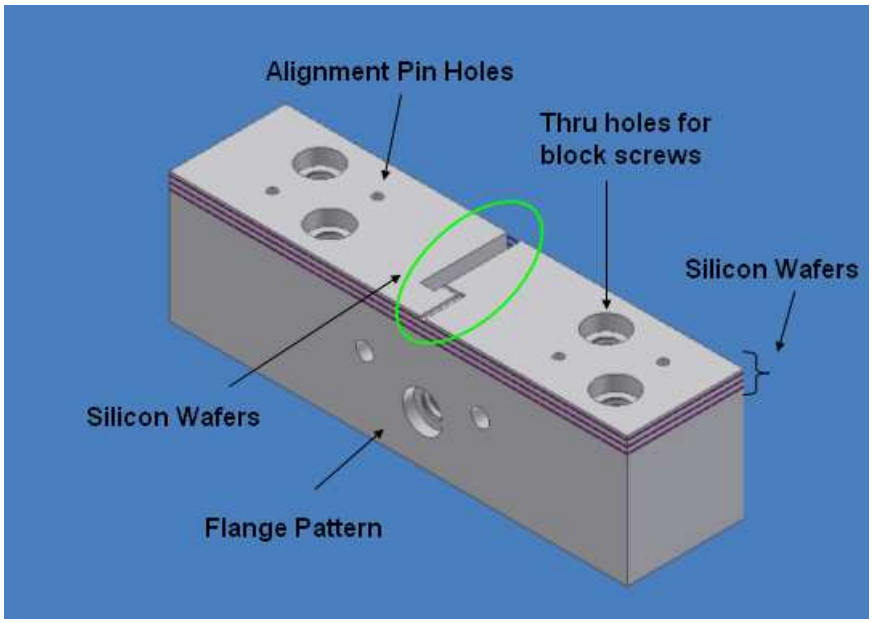

Figure 55: An Autodesk drawing of one half of the multiplier measurement fixture with 3 silicon layers shown..

pieces and that of the fixture. A drawing of one-half the fixture along with three silicon layers is shown in Figure 55. The fixture is made of brass and as seen in Figure 55 has the necessary threaded holes to secure the two halves of the fixture together as one unit. The fixture also had the standard waveguide flange patterned to mate to standard rectangular waveguide. Specific attention was paid to account for the silicon wafer pieces so the waveguide flange pattern would have the appropriate dimensions. A photograph of the assembled multiplier is shown in Figure 56. The waveguide openings are shown in Figure 57 and Figure 58.

4.6 Results

There were two sets of fabrication and measurement for the multiplier block. The first attempt was fabricated with the two middle layers of silicon having a thickness of 300 um. During assembly and measurement it was discovered that using this thickness of wafer yielded pieces that were relatively fragile. Moreover, three different lengths of backshorts were fabricated (see Figure 49) in attempt to achieve a better input match and to couple more power to the diode circuit. The pieces that were the optimal backshort length broke

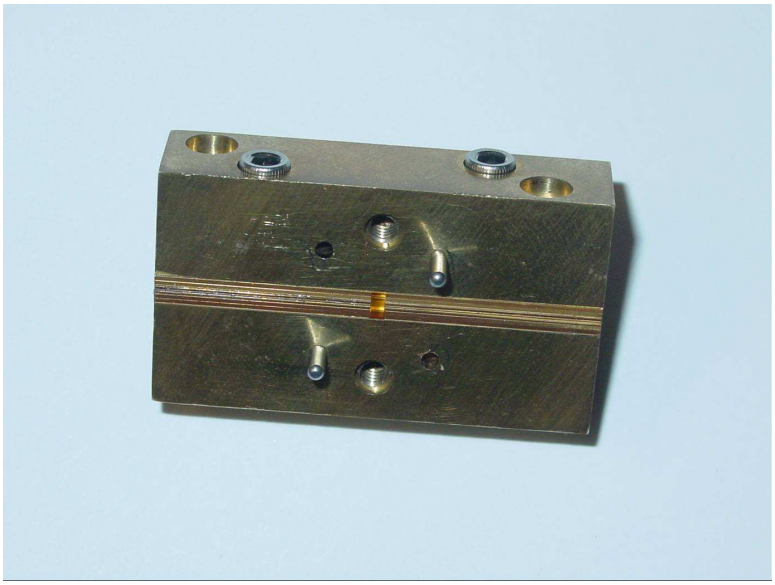

Figure 56: A photograph of the assembled measurement fixture with the six silicon layers installed.

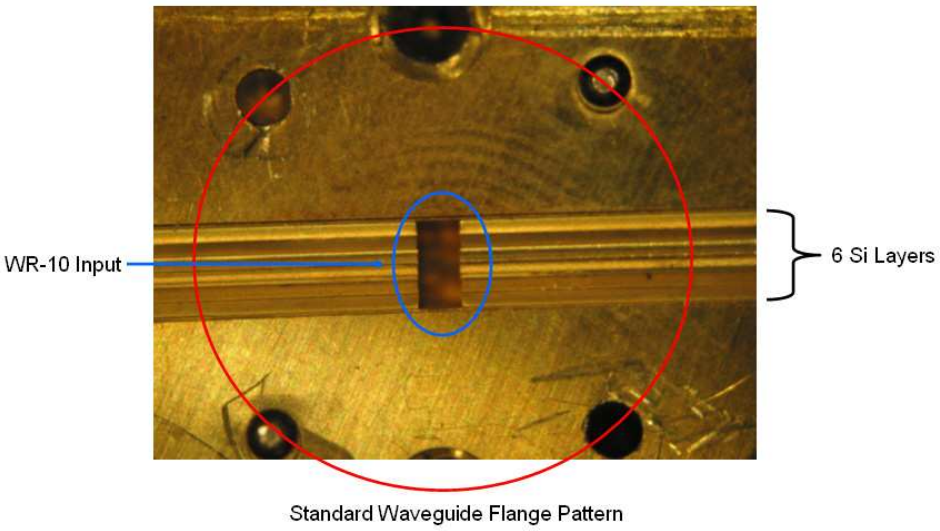

Figure 57: A photograph of the WR-10 waveguide input section of the silicon multiplier.

during assembly. Of the two reaming backshort lengths, only one yielded results.

4.6.1 First Silicon Waveguide Multiplier Results

For the first test, the measurement was started at an input frequency of 90 GHz since it was the maximum output for this multiplier when configured in an all metal block [69]. It was determined during the testing, that the maximum output power frequency had shifted to an input frequency of 93 GHz. This corresponded to an output frequency of

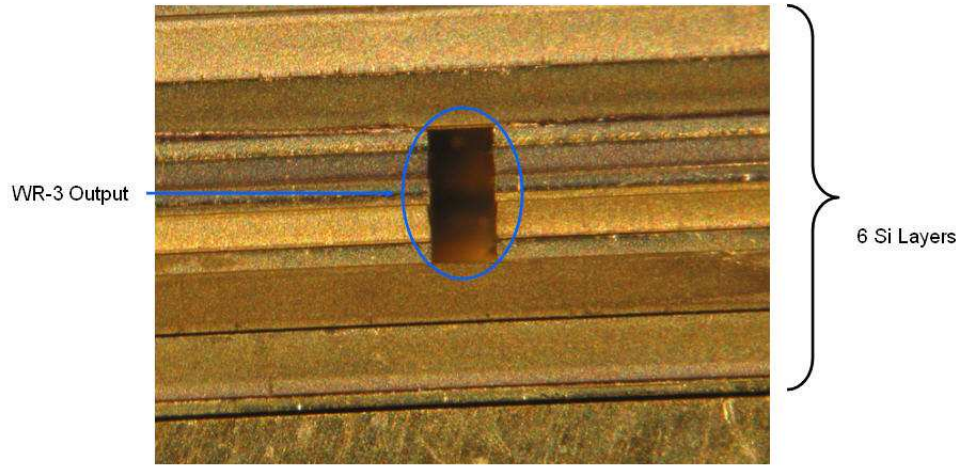

Figure 58: A photograph of the WR-3 waveguide output section of the silicon multiplier.

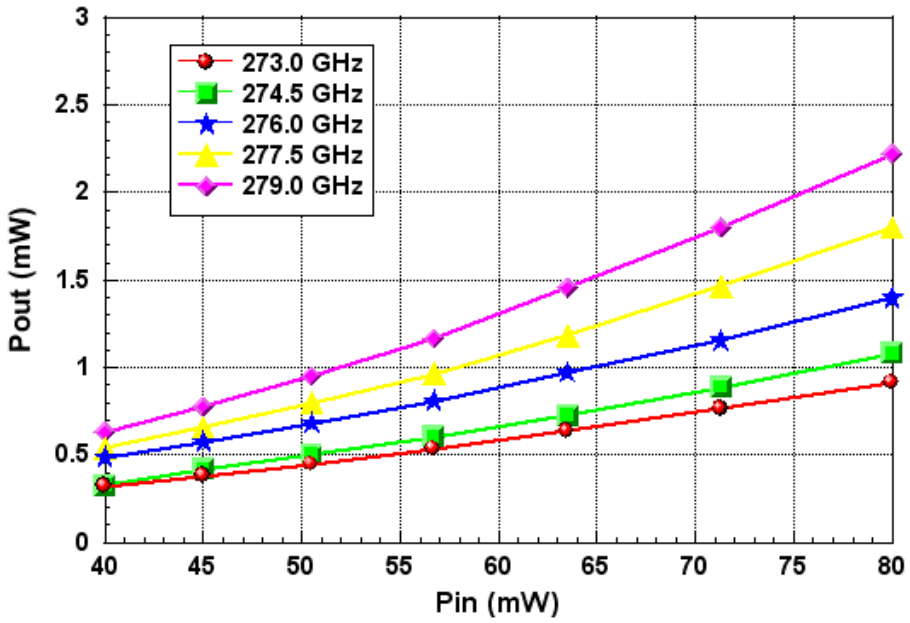

Figure 59: Output power versus input power of the first silicon waveguide multiplier.

279 GHz. This shift in frequency can be attributed to a few conditions. The obvious would be the backshort length. The optimal matching is not archived by using an incorrect backshort length and likely contributed to the frequency shift. The placement of the diode chip inside the channel could also cause a frequency shift. Finally, the composition of the silicon waveguide could also cause a shift since the stacked wafer might not produce planar waveguide walls. The results of this testing are shown in Figure 59-Figure 63. Figure 59

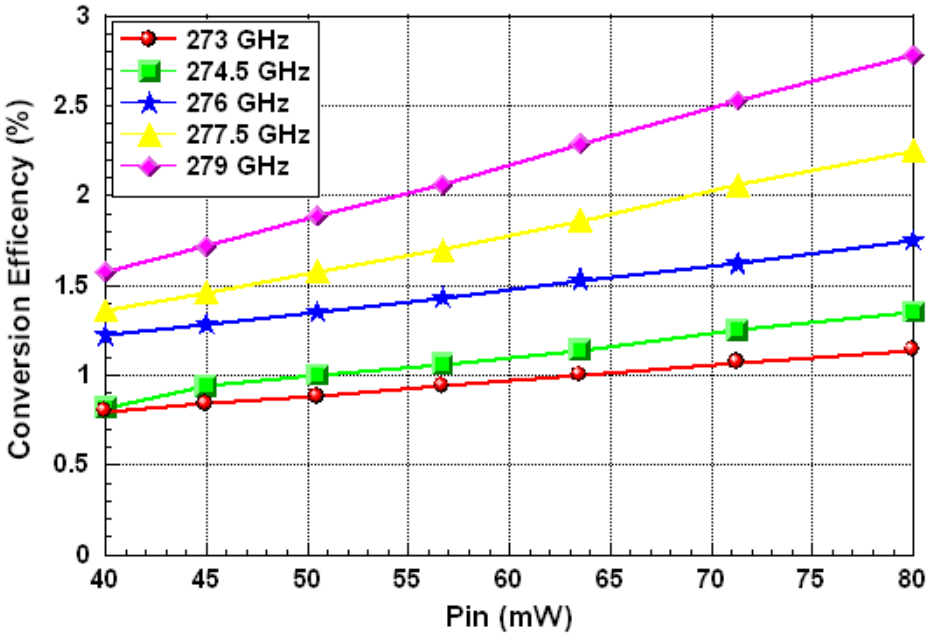

Figure 60: Conversion efficiency versus input power of the first silicon waveguide multiplier.

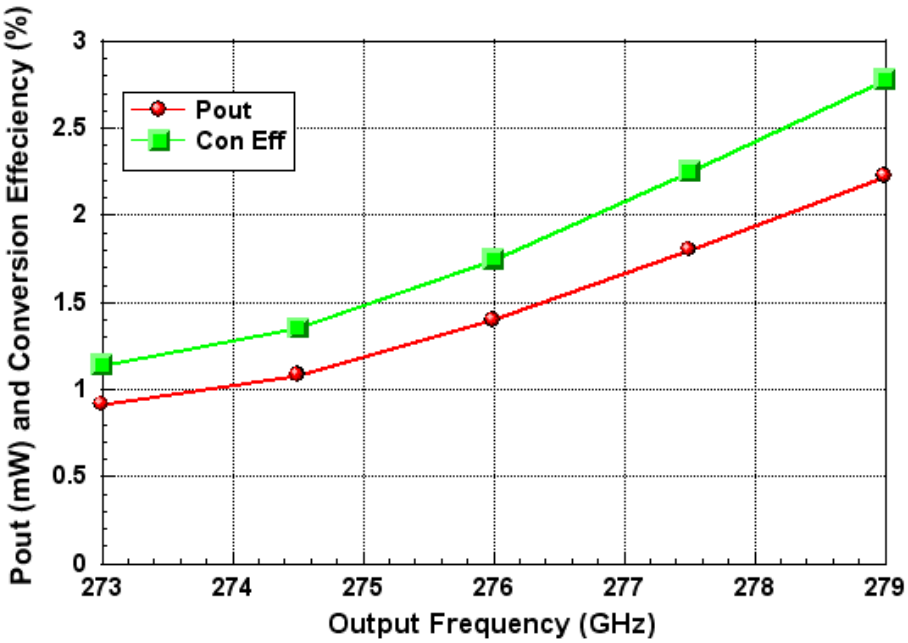

Figure 61: Output power and conversion efficiency versus input power of the first silicon waveguide multiplier.

shows the output power v.s. input power for output frequencies between 273-279 GHz. The maximum output power was determined to be at 2.8 mW at 279 GHz. Figure 61 shows

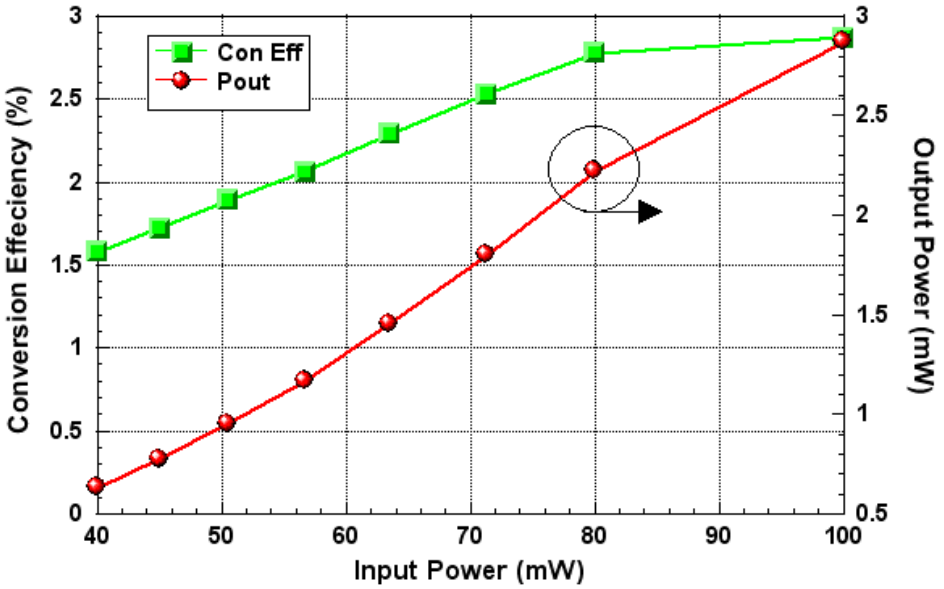

Figure 62: Output power and conversion efficiency versus input power of the first silicon waveguide multiplier at the maximum output power frequency, 279 GHz.

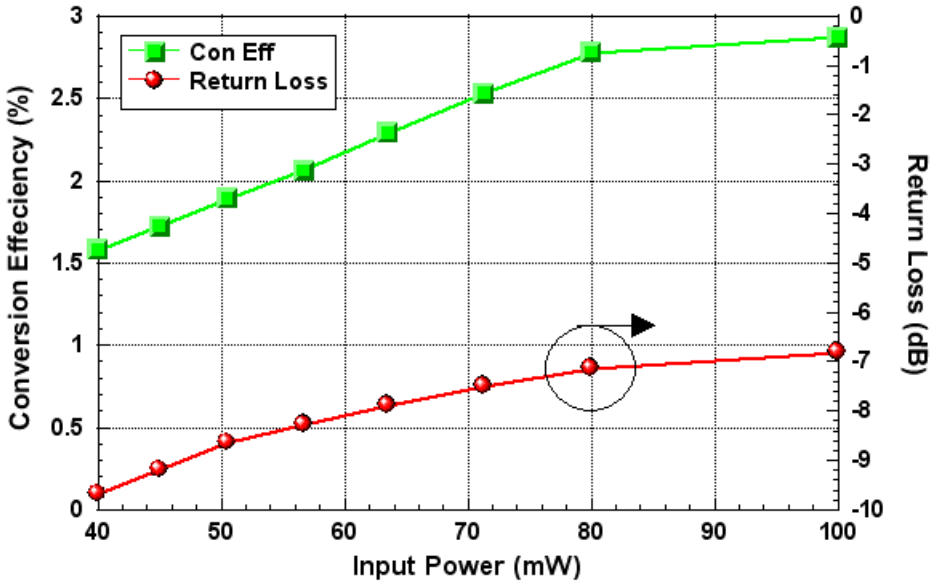

Figure 63: Output power and return loss versus input power of the first silicon waveguide multiplier at the maximum output power frequency, 279 GHz.

the input power v.s. conversion efficiency for the same set of frequencies. As expected, the maximum output power frequency matches the maximum conversion efficiency frequency of 279 GHz. The maximum efficiency is 2.8%. Figure 62 shows the conversion efficiency and output power at the same output frequencies with a constant input power of 80 mW.

Figure 63 shows conversion efficiency and return loss v.s. input power. Unexpectedly, the

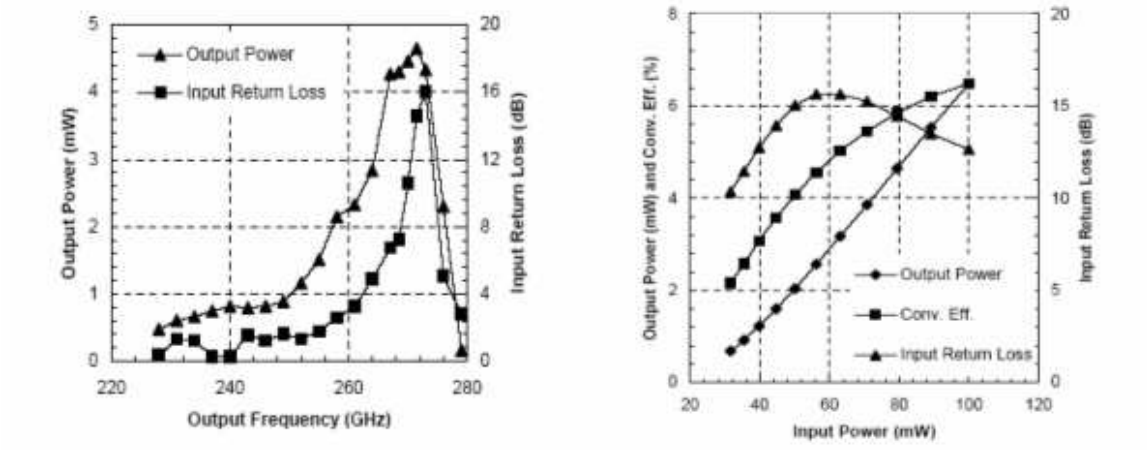

Figure 64: Results of the metal waveguide multiplier block performed by University of Virginia.

return loss degrades as the conversion efficiency improves. The improved return loss is also tied to an increase in output power. While the results are good for this first time that a silicon micromachined waveguide has been used in a multiplier application, the results are below expectations. The results for the multiplier in a brass fixture are shown in Figure 64 and the results are summarized and compared in Table 3. As can be seen in the table, the

Table 3: A comparison of the first silicon micromachined multiplier and the brass block multiplier.

	Si Block 1	Metal Block
Output Freq (GHz)	279	271.5
Output Power (mW)	2.8	6.5
Conv Eff (%)	2.8	7.2
Return Loss (dB)	7	16

results are far below the performance of the brass block.

4.6.2 Second Silicon Waveguide Multiplier Results

An incorrect backshort length was the main contributor to the poor performance of the silicon micromachined waveguide multiplier block. For the fabrication of this multiplier, the entire fabrication would be a single backshort of correct length. Also, the 300 um silicon

wafer was replaced with a 400 um layer to reduce its fragility (see Figure 50) and form a more robust design. Since the wafer change increased the overall thickness of the silicon stack, a new fixture was made so the flange pattern would have the correct dimensions. The measurement results this version are shown in Figure 65-Figure 68. Figure 65 shows

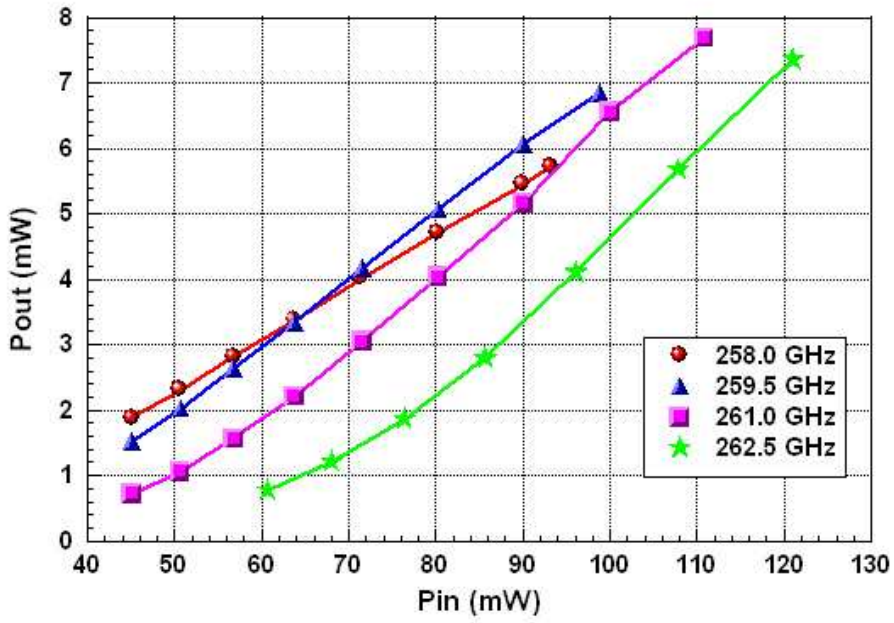

Figure 65: Output power versus input power of the second silicon waveguide multiplier.

a significant power increase over the results of the first measurement. The frequencies of operation have shifted from the previous measurement. This is likely due to the previously discussed possibilities as well as the placement of the diode chip within the waveguide channel. Figure 67 also demonstrates much improved efficiency. Figure 68 shows the conversion efficiency and output power at an output frequency of 261 GHz. Figure 68 shows the conversion efficiency and the return loss at 261 GHz. The results were much improved over the original results. A comparison of these results to the metal block are shown in Table 4. From this comparison, it is evident that a higher output power and better return loss was achieved with a comparable conversion efficiency. This is a strong indication that there is very little difference between the use of a metal block and the silicon micromachined block.

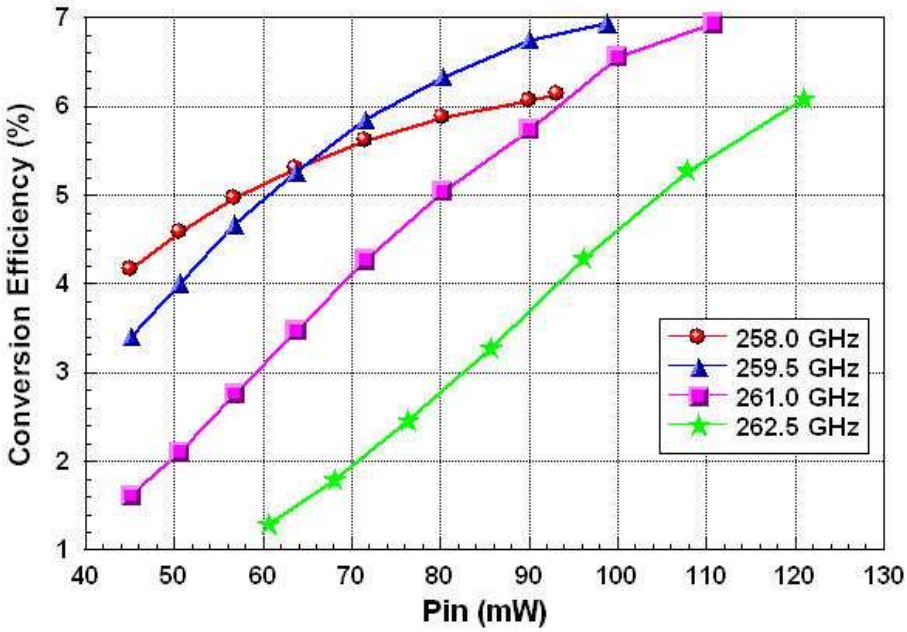

Figure 66: Conversion efficiency versus input power of the second silicon waveguide multiplier.

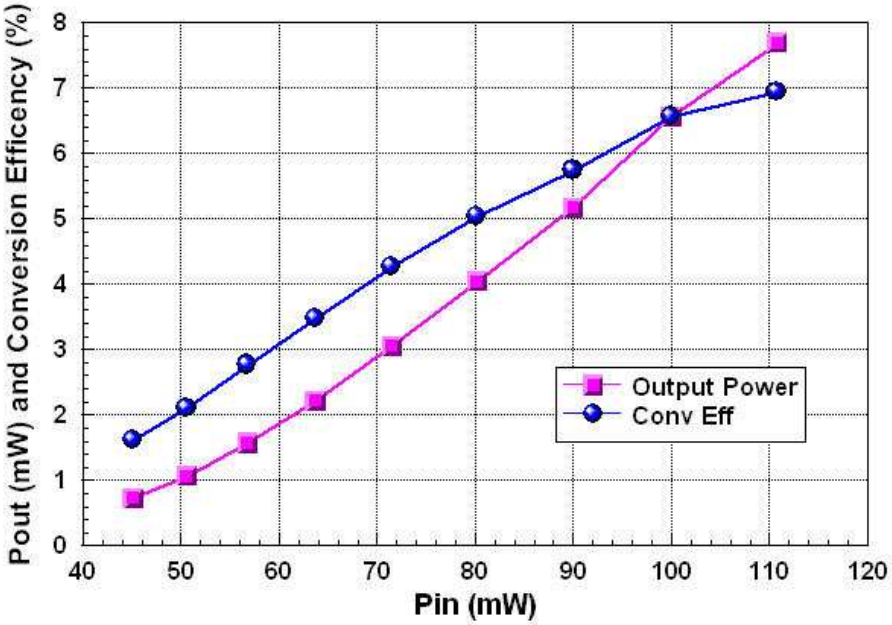

Figure 67: Output power and conversion efficiency versus input power of the second silicon waveguide multiplier at the maximum output power frequency, 261 GHz.

4.7 Summary

In this chapter, a brief review of diodes utilized in multiplier applications above 100 GHz was given. Highlights of the benefits of using an HBV diode were given. An analysis of

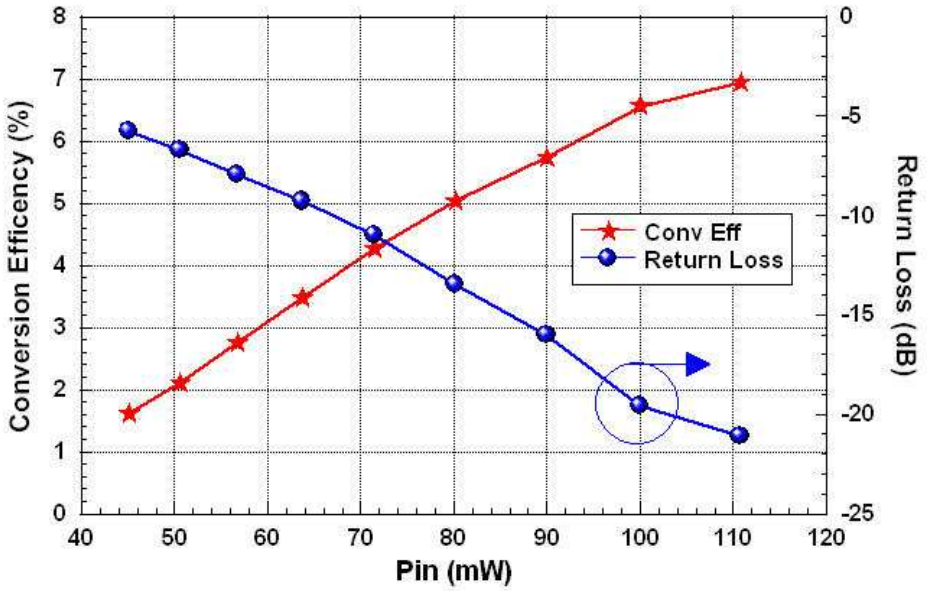

Figure 68: Return loss and conversion efficiency versus input power of the second silicon waveguide multiplier at the maximum output power frequency, 261 GHz.

Table 4: A comparison of the silicon micromachined multiplier and the brass block multiplier.

	Si Block 2	Metal Block
Output Freq (GHz)	261	271.5
Output Power (mW)	7.7	6.5
Conv Eff (%)	6.9	7.2
Return Loss (dB)	21	16

the method of design was covered to form the silicon micromachined rectangular waveguide multiplier block. An extensive review of the measurement setup required to characterize a multiplier of this type was given. A thorough analysis of the fixture utilized for the measurement was also presented. Two different measurements were performed; the second measurement demonstrated excellent performance and showed very little difference between the metal waveguide block and the silicon micromachined block. An output frequency of 261 GHz was generated with an output power of 7.7 mW and efficiency of 6.9% with a return loss of 21 dB. This is the first demonstration of a multiplier utilizing a silicon micromachined based waveguide.

CHAPTER V

COMBINER MULTIPLIER

5.1 Introduction

In this chapter a power combined multiplier utilizing an HBV diode will be covered. A detailed analysis of power splitting and combining for the purpose of implementing two HBV multiplier circuits to generate additional power is presented. The selection of using branch line couplers as the components to handle the power splitting and combining is discussed. In the end, the decision to use a brass block instead of silicon micromachined block is made.

5.2 Power Combining

When the power combining of active devices is considered, there are various choices by which it can be accomplished. Generally speaking, it is done in the way, that the input signal is split, then the split signals are fed through its own active device, and finally the split signals are combined at the output. The method of power combining at the chip level involves multiple active devices connected together by planar transmission lines on the same substrate. These circuits generally share the same matching network. Alternatively, power combining can be done at the circuit level, which uses multiple independent sub-circuits that are generally combined off-chip or using a waveguide. Both, chip level and circuit level power combining are somewhat similar and are represented by the block diagram shown in Figure 69. Lastly, power can be combined using spacial combining. Spatial combining is accomplished using an array of active circuits, by which power is combined in free space rather than directed by a conducting medium. This type of power combing can also be done with a resonant cavity or waveguide to better direct the energy. An example block diagram is shown in Figure 70.

For this work, the same HBV diode fabricated by the University of Virginia used in the

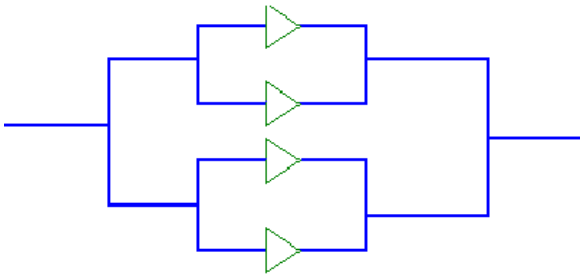

Figure 69: Block diagram demonstrating both chip level and circuit level combining.

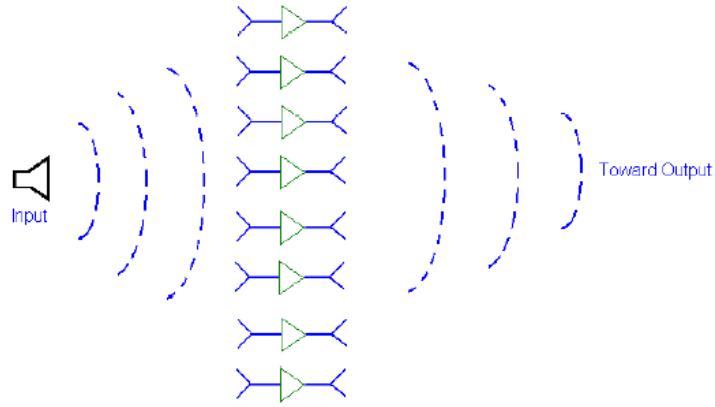

Figure 70: Block diagram demonstrating spatial combining.

single multiplier are used. Since this diode already has a circuit level matching network, circuit level power combining can not be utilized. The circuit design of spatial power combining is significantly complex and is not suitable for this research work. The most suitable and feasible type of power combing for this application would be at the circuit level using waveguide components.

5.3 Ideal Combiner Study

In order to ascertain the appropriate type of power splitting and combining, the initial study is done using the ideal components. To accomplish this, a base line comparison is needed to evaluate how well the power splitting/combining is performing. The input power split is considered in detail. The drawing of the schematic is shown in Figure 71. The input section of the multiplier block is simulated in Ansoft's HFSS. The simulated circuit consists of a waveguide input (port 1) WR-10, and a shallow channel where the microstrip circuit is placed (port 2). The microstrip protrudes into the waveguide to pick up the

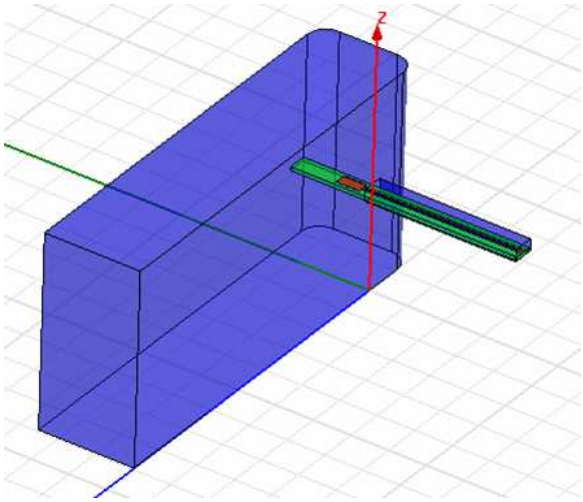

Figure 71: HFSS setup of the input section of the multiplier.

incoming signal from the waveguide. The simulated results are shown in Figure 72. As in Figure 72, the left plot shows the efficient coupling (S21) from the waveguide to the microstrip, and the impedance matching (S22) presented to the diode is shown in at the right plot. In the ideal case, the power divider provides a sufficiently good match, such that

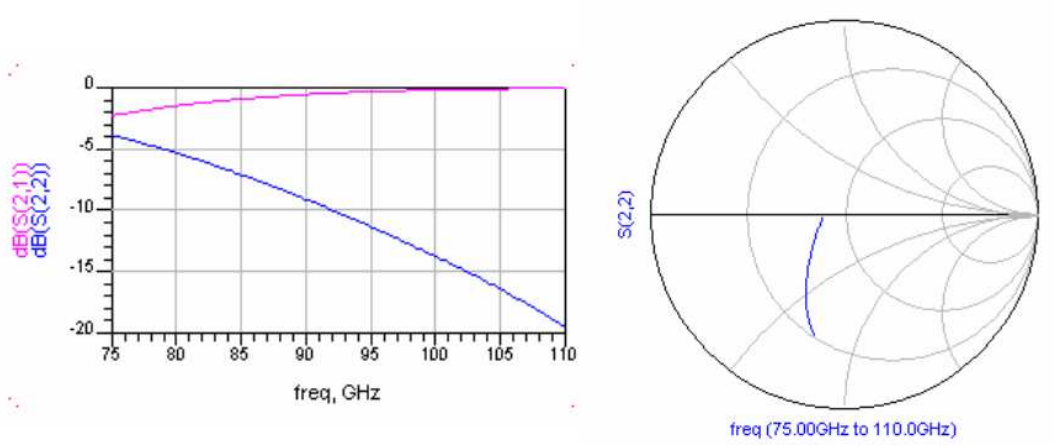

Figure 72: S-Parameters of the input section of the multiplier. S22 is the input of the microstrip section.

the impedance presented to the diode remains as close as possible to the base line. To carry out the analysis, the full wave S-parameters from HFSS are imported into Agilent's ADS. Two copies of these S-parameter files are placed in the schematic, and the terminations are placed at the microstrip ports. Since the ideal power splitter allows control of the isolation

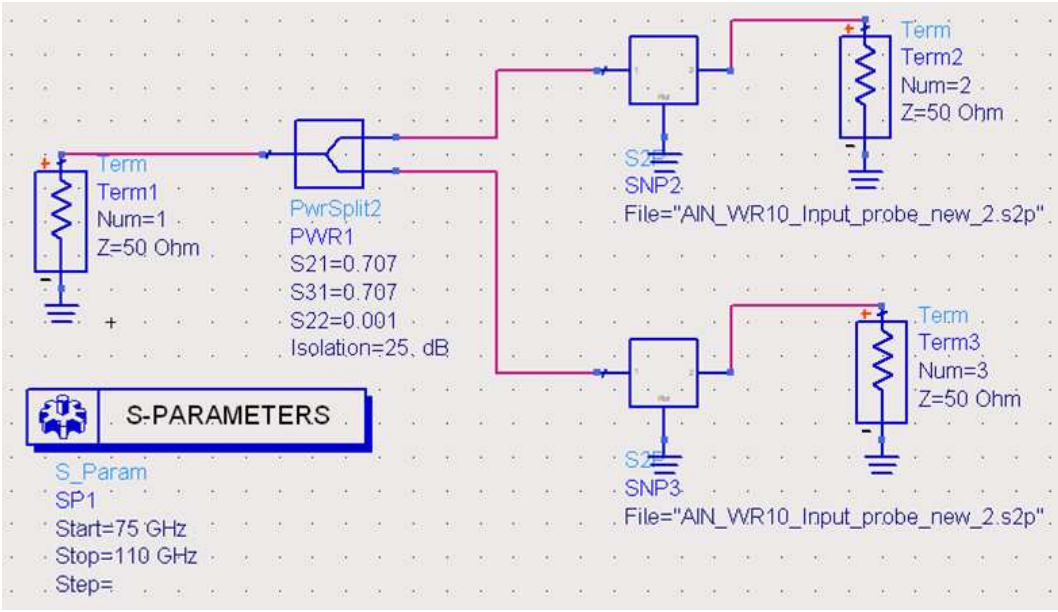

Figure 73: ADS setup for the ideal case of combining the inputs of two multipliers.

between the split ports and the matching at all three ports, it is placed with each of the split ports attached to the waveguide port of the input of the multipliers section. The schematic of this circuit is shown in Figure 73.

The initial simulation demonstrates a very ideal case where the matching at the split ports is -60 dB and the isolation between the split ports is 25 dB, as shown in Figure 74. In Figure 74, the simulated results with the ideal splitter and from the single multiplier is indistinguishable. To get a good understanding of the impact of each parameter, the isolation and the matching parameters are be varied independently, with some realistic values in consideration.

5.3.1 Varying the Power Splitter Matching Parameter

The input of a single multiplier is composed of a WR-10 waveguide and is presented with a good match with the utilized measurement equipment. Thus, to achieve a comparable result with that of a songle multiplier the power splitter utilized needs to provide a good impedance match to the input of a single multiplier. Since an ideal impedance matching of -60 dB is unrealistic, the ideal power splitting impedance matching is varied from -30 dB to -15 dB to investigate the impact of mismatch, with the isolation parameter initially

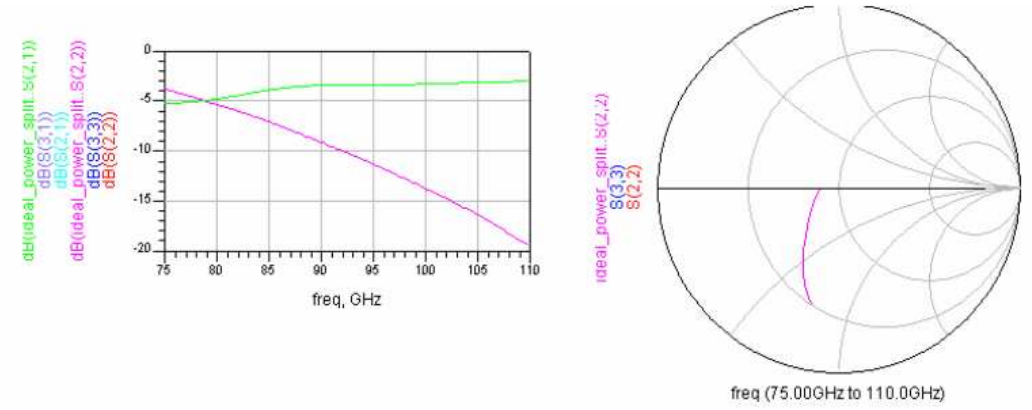

Figure 74: Simulation results for ideal splitter with the isolation set at 25dB and the reflection coefficient at -60 dB.

maintained at 25 dB. The results are shown in Figure 75-Figure 78.

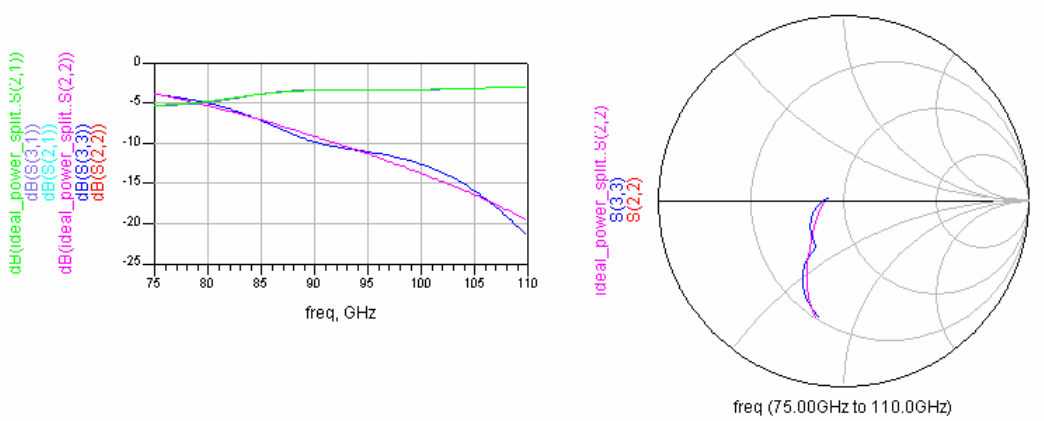

Figure 75: The simulated results for ideal power splitter with the isolation parameter fixed at 25dB and the impedance matching parameter at -30 dB.

It can be seen from Figure 75 and Figure 76, when the impedance match is reduced from -30 and -25 dB, there is very minimal impact. When it is further reduced to -20 and -15 dB, as shown in Figure 77 and Figure 78, a more pronounced deviation between the power splitter and base line is visible. The simulations demonstrate that the impedance match of -20 dB and above is required between the power splitter and the single multiplier, in order to preserve the impedance match of the next level sub-circuits.

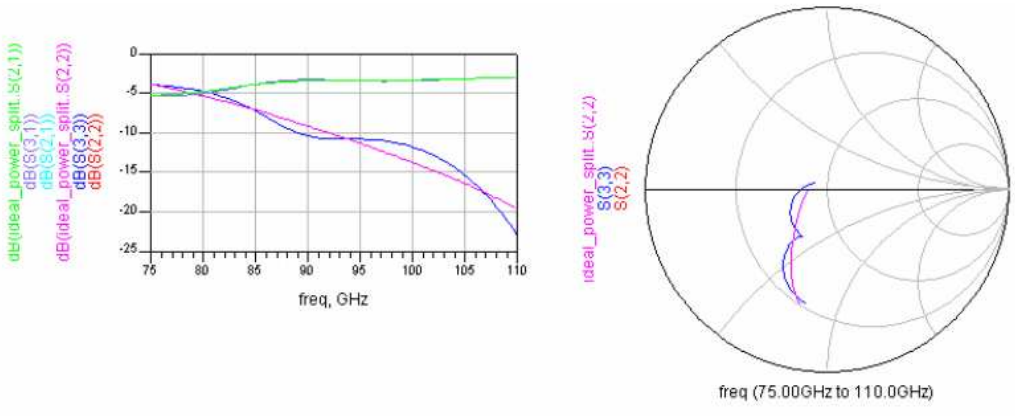

Figure 76: The simulated results for ideal power splitter with the isolation parameter fixed at 25dB and the impedance matching parameter at -25 dB.

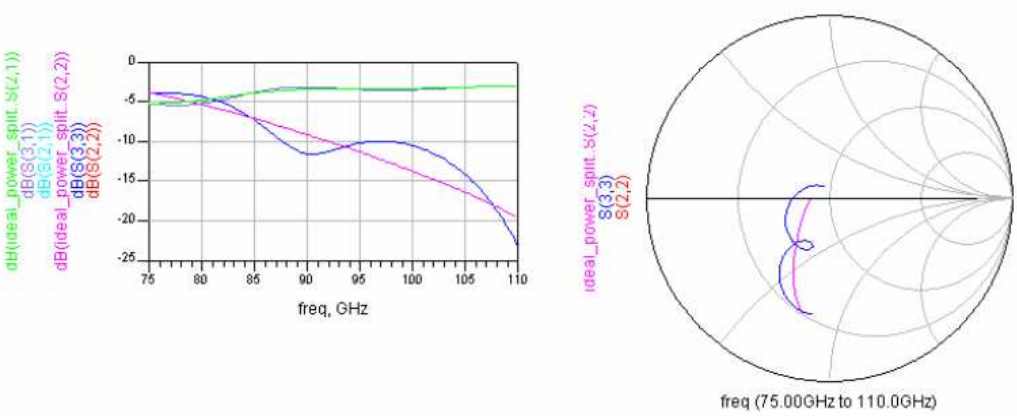

Figure 77: The simulated results for ideal power splitter with the isolation parameter fixed at 25dB and the impedance matching parameter at -20 dB.

5.3.2 Varying the Power Splitter Isolation Parameter

In this section, the impact of the isolation parameter is studied and initially, this is the only parameter varied in the analysis. This will allow for the insight into how much isolation is needed to maintain a good match for the diode.

In this study, the impedance match between the power splitter and the input to the multiplier is maintained at -60 dB, to eliminate the cross effects of both parameters.

The results are shown from Figure 80 to Figure 82. As in Figure 80, when the isolation is reduced to 10 dB, some noticeable impact can be seen from the Smith chart. In Figure 81, when the isolation is further reduced to 7 dB, the more pronounced resonances can be

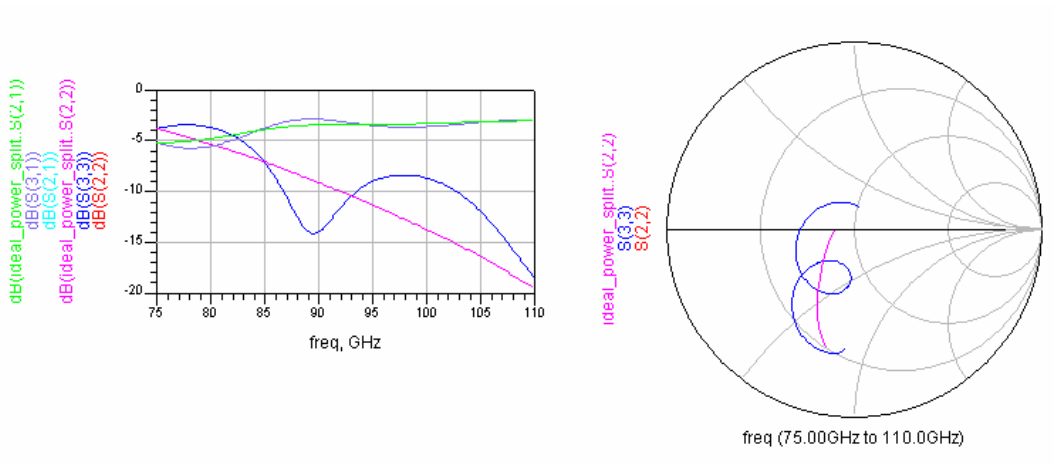

Figure 78: The simulated results for ideal power splitter with the isolation parameter fixed at 25dB and the impedance matching parameter at -15 dB.

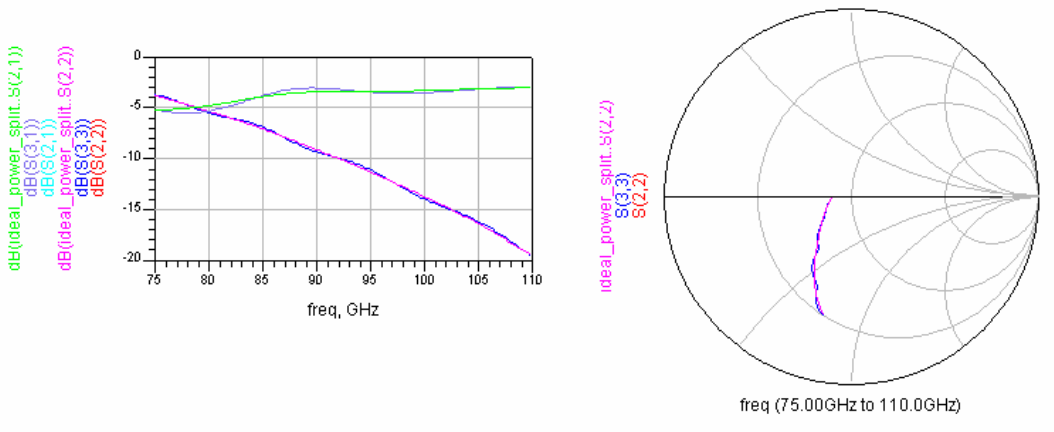

Figure 79: The simulated results for ideal power splitter with the isolation of 15 dB and the impedance matching parameter at -60 dB.

observed.

Figure 82 shows the result when the isolation is further reduced to 4 dB it can be seen, that the resonances are very large and the impact is detrimental to the performance of the overall power combiner.

5.3.3 Composite of Isolation and Impedance Match Variation

In this study, both the isolation and impedance match of the power splitter are considered. The simulated results of an isolation of 13 dB and a splitter port impedance match of -20 dB are shown in Figure 83.

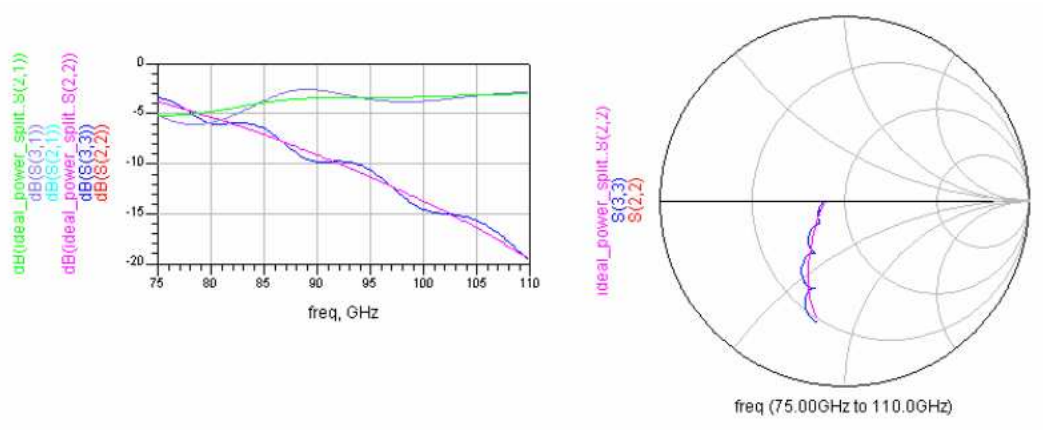

Figure 80: The simulated results for ideal power splitter with the isolation of 10 dB and the impedance matching parameter at -60 dB.

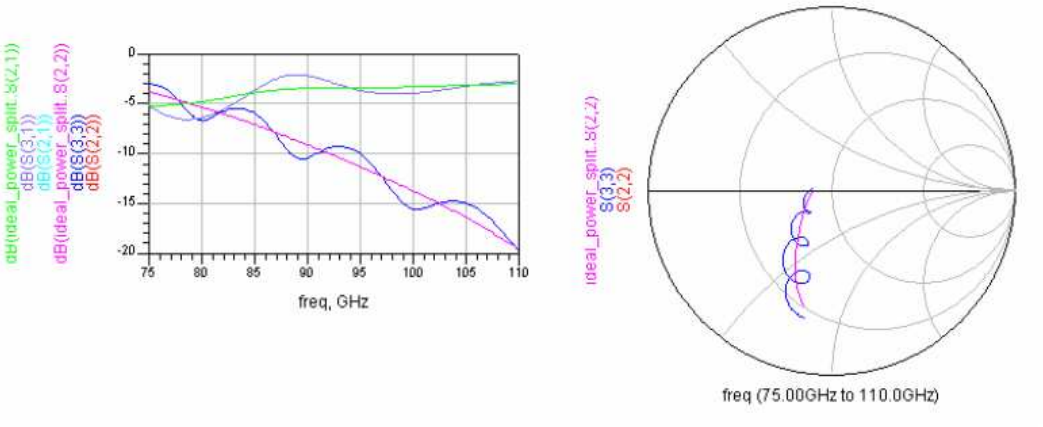

Figure 81: The simulated results for ideal power splitter with the isolation of 7 dB and the impedance matching parameter at -60 dB.

As shown in Figure 83, the impact of a non-ideal power splitter is clearly distinguished from the ideal case, which shows strong resonances in the Smith chart. Another study is done with the isolation of 4 dB and the plit port impedance match of -20 dB, and the results are shown in Figure 84. Figure 84 shows several resonances indicating a severe degradation of the impedance, which ultimately leads to an unacceptable performance or non-functioning waveguide circuits.

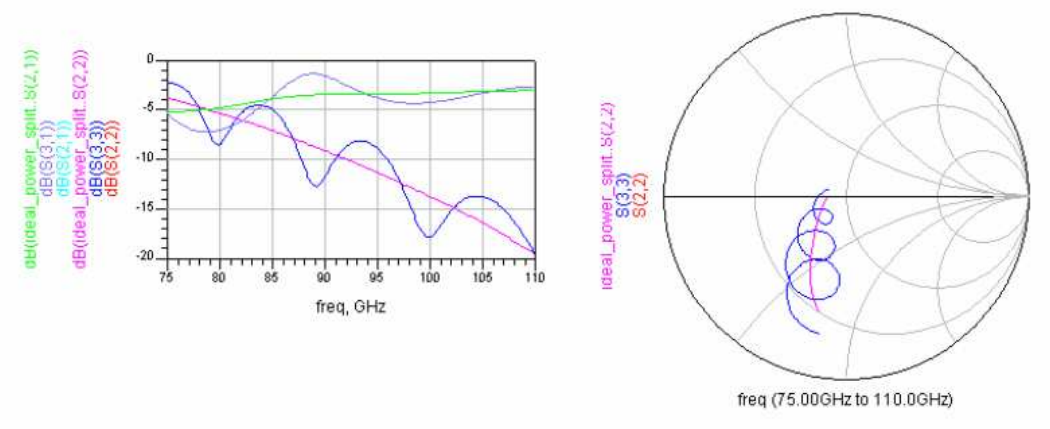

Figure 82: The simulated results for ideal power splitter with the isolation of 4 dB and the impedance matching parameter at -60 dB.

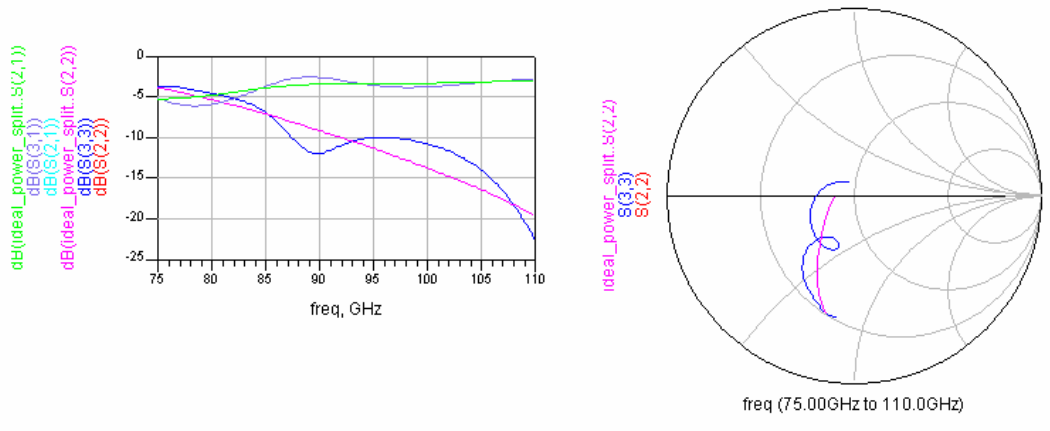

Figure 83: The simulated results for ideal power splitter with the isolation of 13 dB and the impedance matching parameter at -20 dB.

5.4 T-Junction for Power Splitting

By far the simplest approach for power splitting is to use a simple waveguide T-junction power splitter, or T-splitter. The T-splitter provides the equal power splitting generally over the entire operating bandwidth of a waveguide frequency. The downside of this type of circuit is it provides very little isolation between the two split ports, which makes it not suitable for this application as shown in the analysis in sections 5.3.2 and 5.3.3. Moreover, all three ports of this component can not be matched to the same impedance, which is required as the port impedance of the input/output waveguide. In other words, if the two splitter ports impedance is matched the input port of the power splitter will have to be

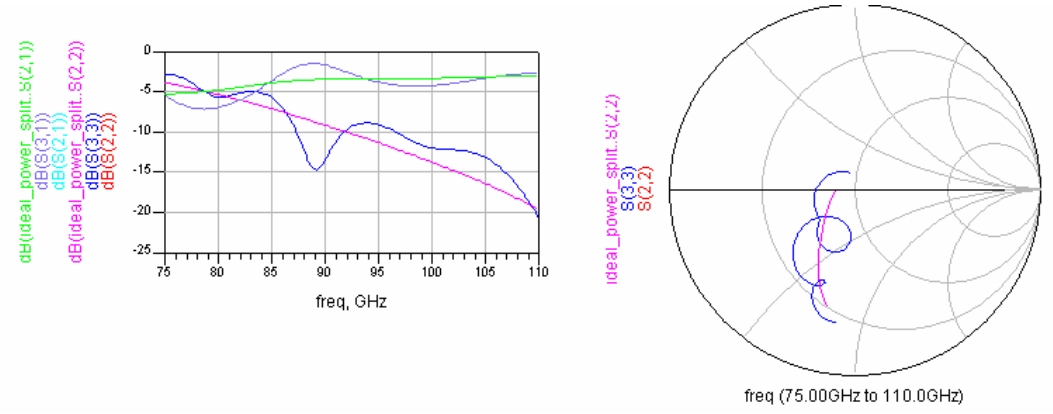

Figure 84: The simulated results for ideal power splitter with the isolation of 6 dB and the impedance matching parameter at -20 dB.

poorly matched, which will degrade the power splitter performance.

To prove this and also verify the T-splitter characteristics, the simulation of such circuit is done using HFSS. The layout for the T-splitter is shown in Figure 85 [28]. This splitter is folded over, which will provide a better mechanical layout for the inclusion of two multipliers. The performance of this T-splitter is shown in Figure 86, which shows a good input impedance match. Also the power split is very flat and equal (S21 and S31). The output match or the match at the split ports is very poor, approximately -8 dB. The isolation is equally poor between the splits on the order of 8 dB.

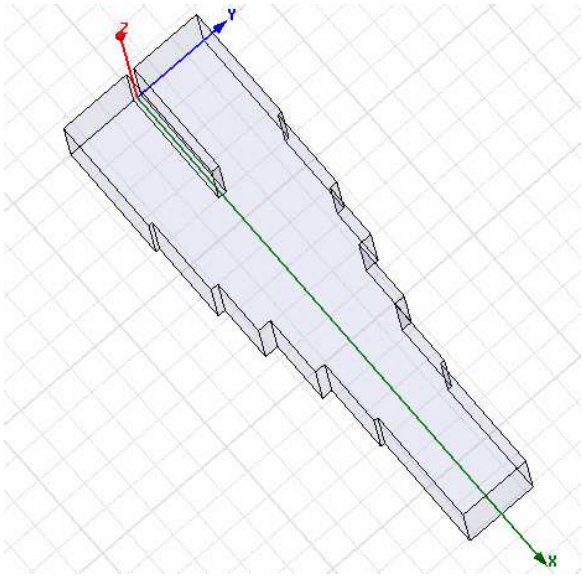

Figure 85: HFSS schematic for the simulation of a simple T-splitter.

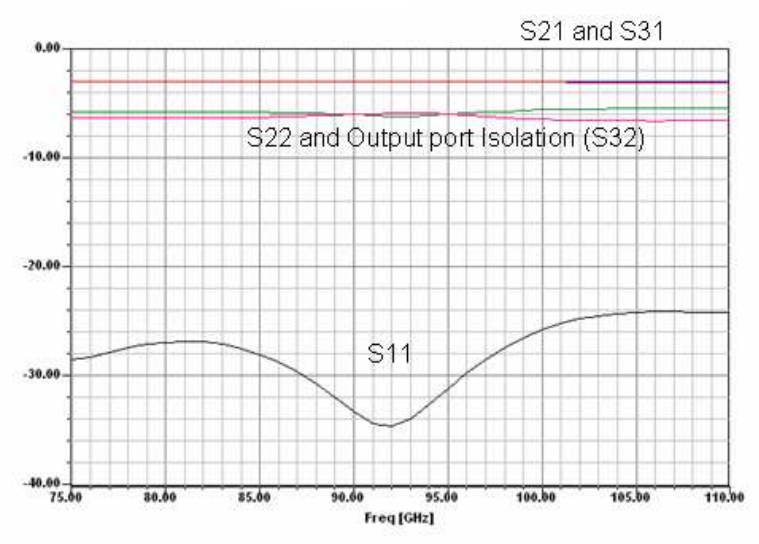

Figure 86: S-parameter results for the T-splitter for reflection and power division.

The S-parameters from HFSS were then exported to ADS for a schematic level analysis. The two split ports were each connected to a multiplier S-parameter data file and the impedance match was examined. The results are shown in Figure 87. As in Figure 87, the split port impedance shows a complete mismatch, which will lead to a very poor or unacceptable power splitting performance.

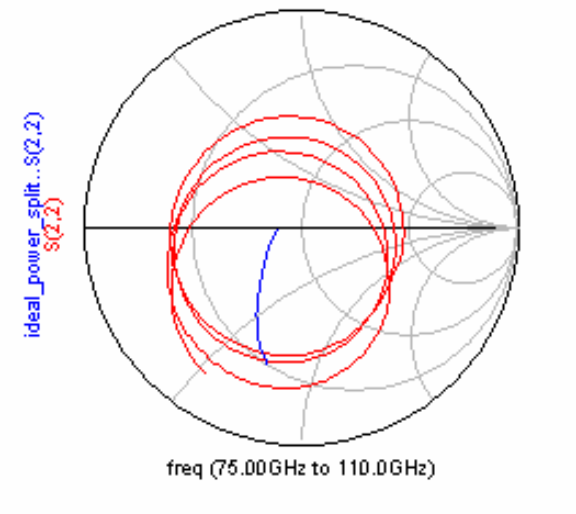

Figure 87: The results of the T-splitter split port impedance match with a multiplier at each of the split ports compared to the impedance match of a single multiplier.

5.5 Waveguide Coupler as a Power Splitter

The analysis of the T-splitter in section 5.5, shows that the power splitter used for this application is required to have a good isolation of 15 dB and impedance match of -20 dB and above. The analysis also shows a 3-port device, such as a T-splitter is not a good candidate for this application unless some substantial modification is made to the devices, such as the inclusion of material to increase the amount of isolation. Comparing a 3-port device like a T-splitter to a 4-port device is more suitable for this power splitting application purpose. A four port device allows for power splitting, equal or unequal, to the split ports, while providing substantial isolation with all ports matched to the same impedance. There are two popular options that can both serve the purpose, a magic Tee and a waveguide coupler. An example of a WR-62 magic tee is shown in Figure 88. Although this could make a suitable component for power splitting/combining, its fabrication becomes an obstacle for farther pursuit of this option. Among the different waveguide couplers, a branchline coupler is a good candidate because of its high isolation between the split ports. can be difficult especially when dimension become small. A suitable alternative is a branch line coupler.

Figure 88: An example of a Magic-T.

A W-Band coupler has been designed and analyzed by the author [29] and the schematic is shown in Figure 89. The coupler was optimized over a bandwidth of 87-92 GHz which represents the previously measured input frequencies to a single multiplier. The reflection coefficient at each port of the coupler and the isolation between the split ports is shown in

Figure 90. As shown in Figure 90, the reflection coefficient is below -23 dB along with the isolation of the split ports. This provides a good impedance match as sufficient isolation between the split ports. The power splitting results are shown in Figure 91. As shown in Figure 91, the split power of the two ports is close to each other at the interested frequency range.

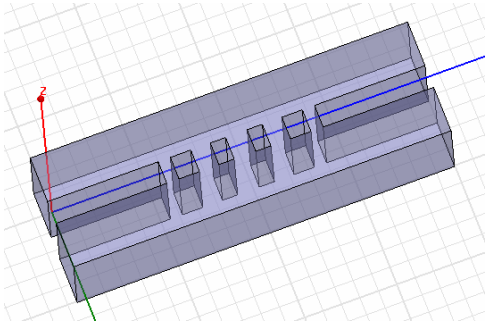

Figure 89: The layout of the W-Band branchline coupler constructed in HFSS.

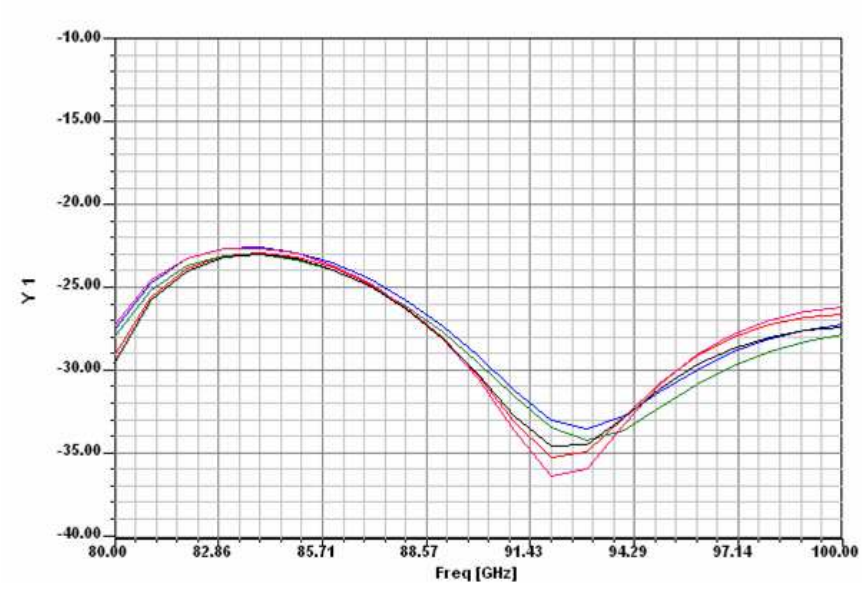

Figure 90: The simulation results of the reflection coefficient at all four ports and the isolation between the split pots of the W-band branch line coupler.

In order to correctly represent the W-band branchline coupler utilized in this design, the entire input structure is constructed in HFSS, as shown in Figure 92. This layout includes the W-band coupler with added length on the input and isolated ports for assembly purposes, also included in the layout are two multiplier input sections representing a realistic

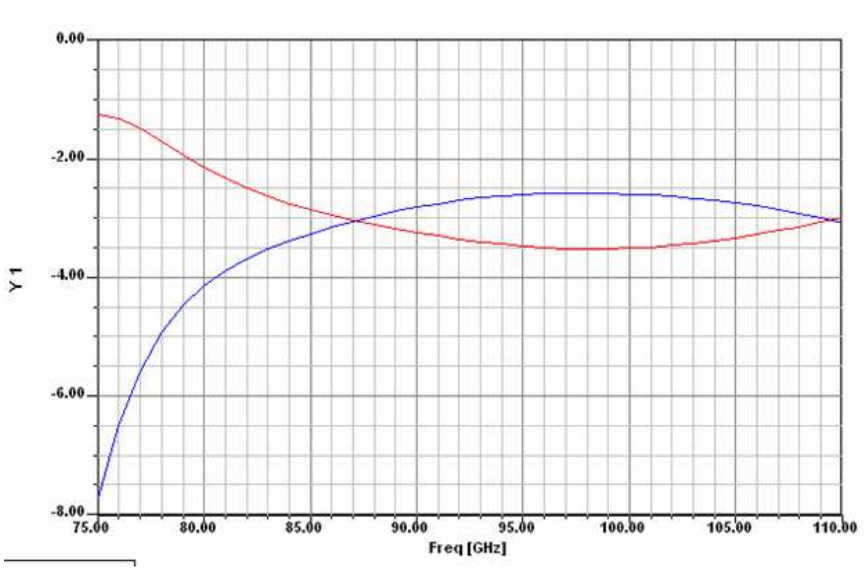

Figure 91: The simulated results of the power splitting at the two split ports of the W-Band branchline coupler.

machined structure. The simulated results in comparison with the ideal case are shown in Figure 93. As shown in Figure 93, the top left plot shows a comparison of the forward transmission from the input of the coupler to the microstrip port. The coupler shows a relatively good agreement to the ideal case; The top right plot shows the reflection coefficient at the microstrip port, which also shows a relatively good match; The bottom left plot shows the reflection coefficient at the input of the coupler which is better than -25 dB over the interested bandwidth; Lastly, the bottom right plot shows the impedance match at the microstrip port which is presented to the diode. There is a very good match between the ideal case and the coupler composite. This designed waveguide branchline coupler represents a good component to be utilized in the construction of a power divided/combined multiplier.

5.6 Waveguide Coupler as a Power Combiner

The output section of the multiplier is similar in nature to the input section. After the signal is fed through the diode for frequency multiplication, it is necessary to transfer the signal path from microstrip to waveguide. The signal is fed through a microstrip to a probe which protrudes into the output waveguide, providing the transition from microstrip to waveguide. The output waveguide is WR-3 (0.864 X 0.432 mm) which also consists of a

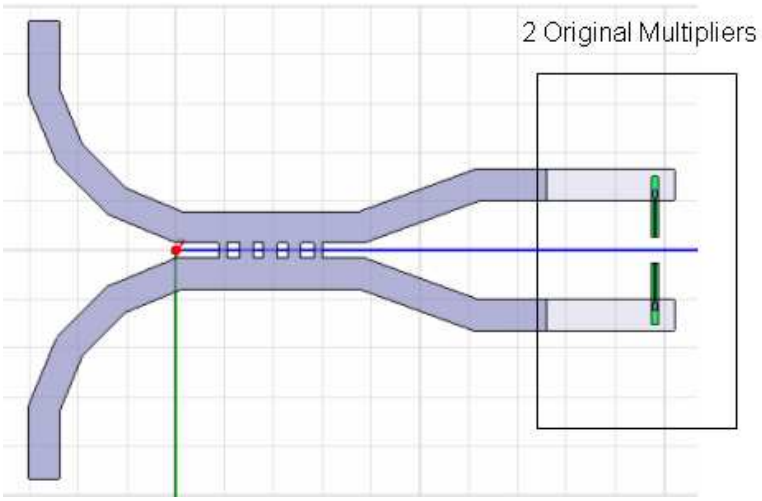

Figure 92: The layout of the W-band brnachline coupler constructed in HFSS, with the two split ports connected to two multiplier input sections.

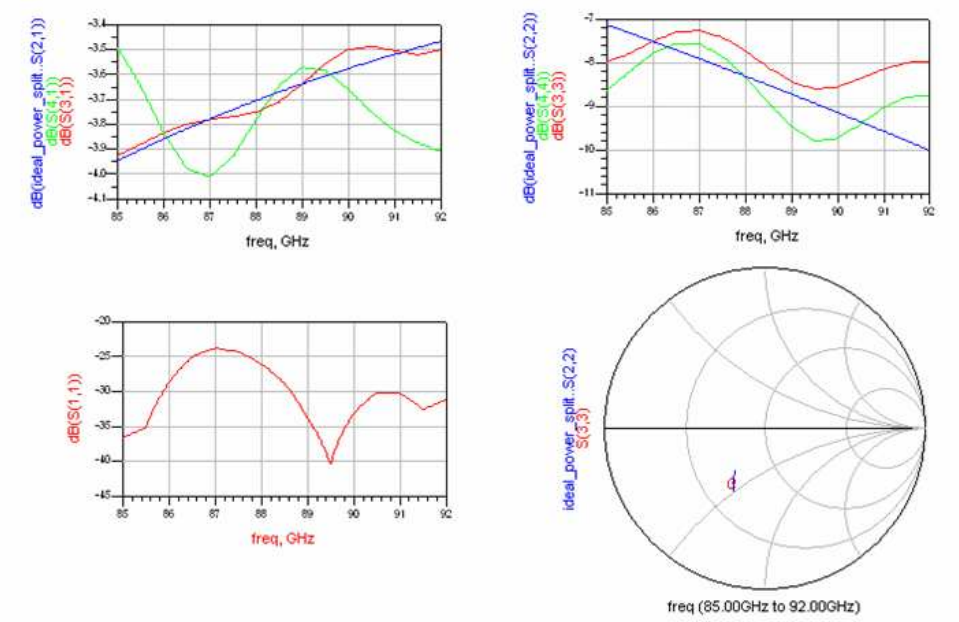

Figure 93: The simulation results of the composite of W-band coupler and multiplier sections. The top left is the forward transmission from waveguide to microstrip; the top right is the reflection coefficient at the microstrip ports; the bottom left is the input reflection coefficient to the coupler; the bottom right is the impedance match at the microstrip port.

back short section for tuning purpose. This section was constructed in HFSS as shown in Figure 94. The simulated S-parameter results of this output waveguide are shown in Figure 95. As shown in Figure 95, the results show that this section of the multiplier efficiently transfers a signal over large bandwidth with a relatively good match.

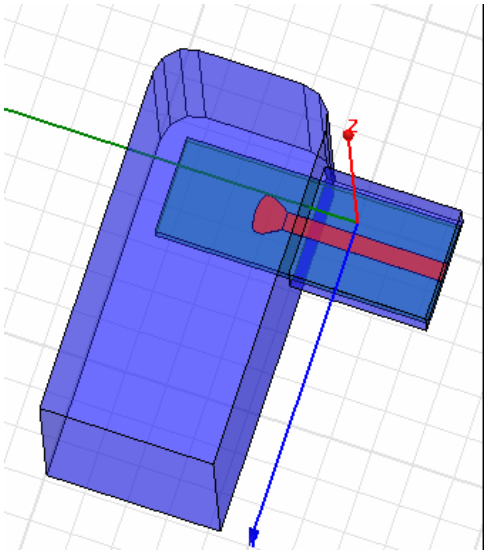

Figure 94: The layout output section of the multiplier constructed in HFSS.

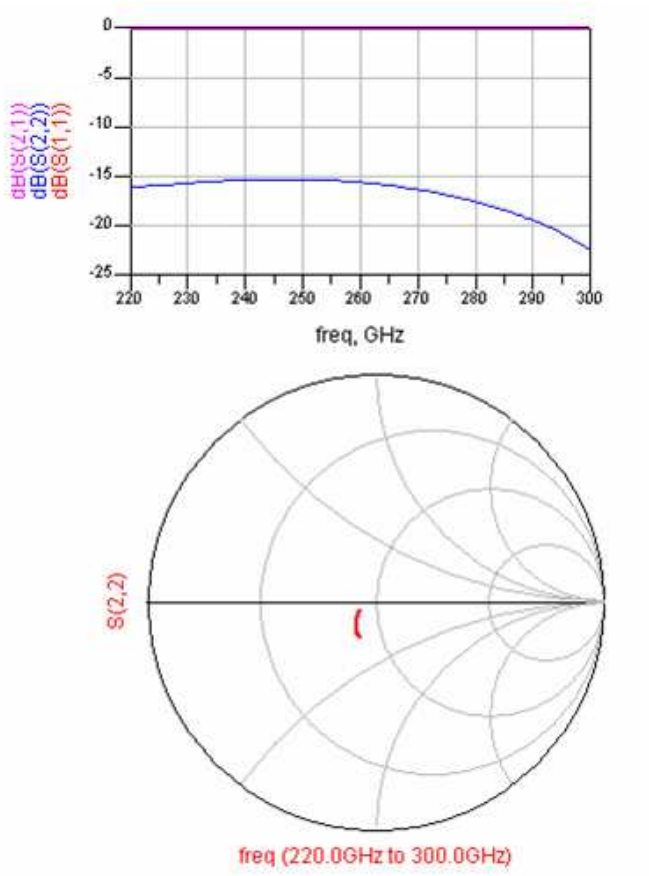

Figure 95: The simulated results of the output section of the multiplier. The Smith chart represents the impedance match presented to the output of the diode.

Similarly as in W-band,a T-splitter is also not the right candidate for this application. A branchline coupler is also utilized, but it functions as a power combiner. The WR-3 branchline coupler was designed and optimized using HFSS [29], and the layout is shown in Figure 96. In Figure 96, it shows the results of the reflection coefficient at each port along with the isolation between the split ports. For both couplers, the phase between the input port and forward transmission port is zero degrees, and the input port is 90 degrees. When these couplers are connected in series, one split will be the difference port have the two signals 180 degrees out of phase, and the other split port will be the sum port with the two signals will be in phase and added together. The simulated results of the power combining are shown Figure 98 with 3 dB representing perfect power combining.

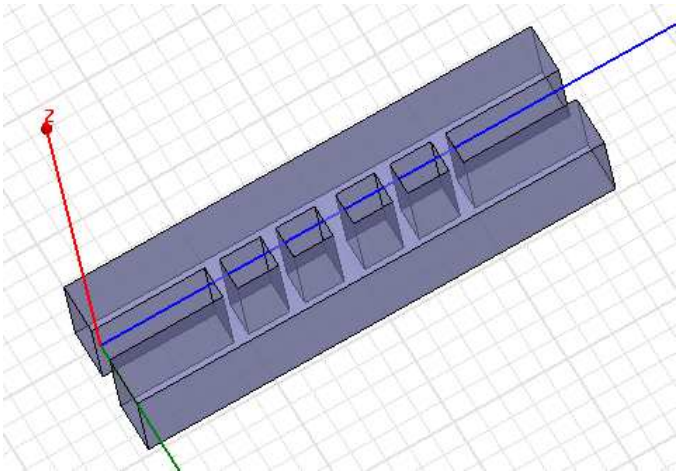

Figure 96: The HFSS schematic of the WR-3 coupler.

The complete analysis of the output coupler with connection to the output multiplier section is then performed in Agilent's ADS. The S-parameters of both the WR-3 branchline coupler and the multiplier output section are imported into ADS. The ADS schematic is setup such that the output of the two multipliers is fed into the WR-3 coupler and the isolated port of the coupler is terminated. The ADS schematic is shown in Figure 99. The compilation is evaluated in a two step process. First, the effectiveness of the combining is analyzed. In order to properly evaluate the combining, a signal must be fed in the multipliers 90 degrees out of phase. To accomplish this, an ideal hybrid coupler is used in ADS to provide the necessary power split and phase shift.

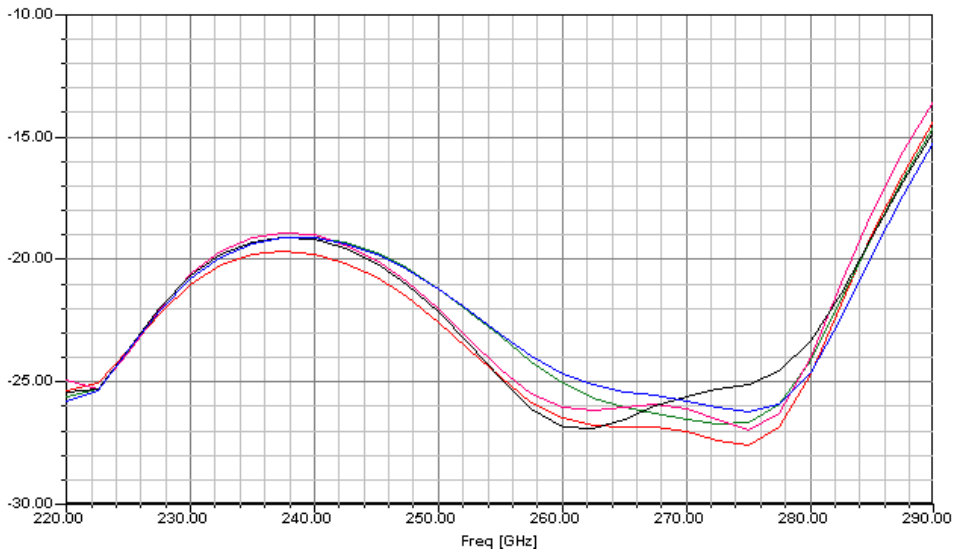

Figure 97: The simulation results of the WR-3 coupler. The reflection coefficient at each port along with the isolation between the split ports.

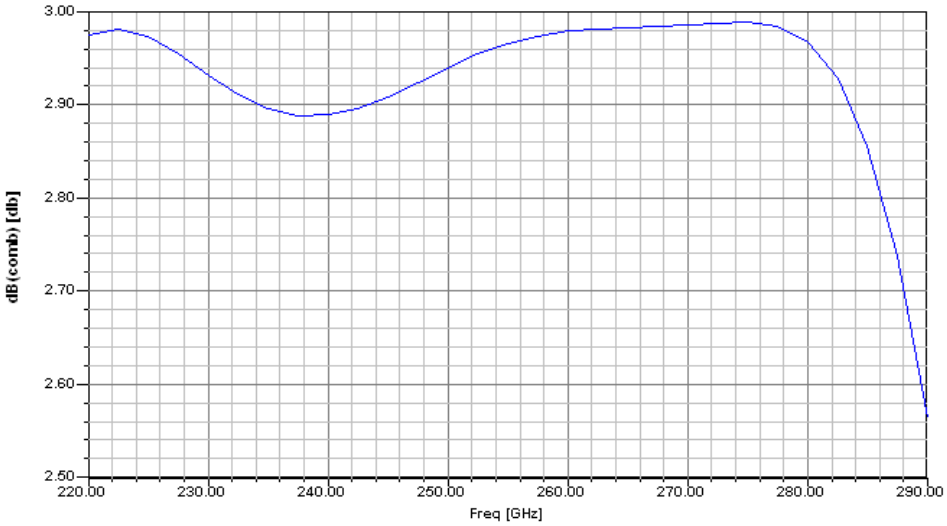

Figure 98: The simulation results of the WR-3 coupler. The combining performance is displayed where 3 dB is perfect combining.

The results of the power combining are shown in Figure 100. As is Figure 100, it shows a very good response of less than 0.2 dB of loss over the 260-270 GHz band of interest. For the isolated port of the coupler, the simulated result is shown in Figure 101. As in Figure 101, a better than 30 dB of cancelation is demonstrated at the isolated port of the coupler.

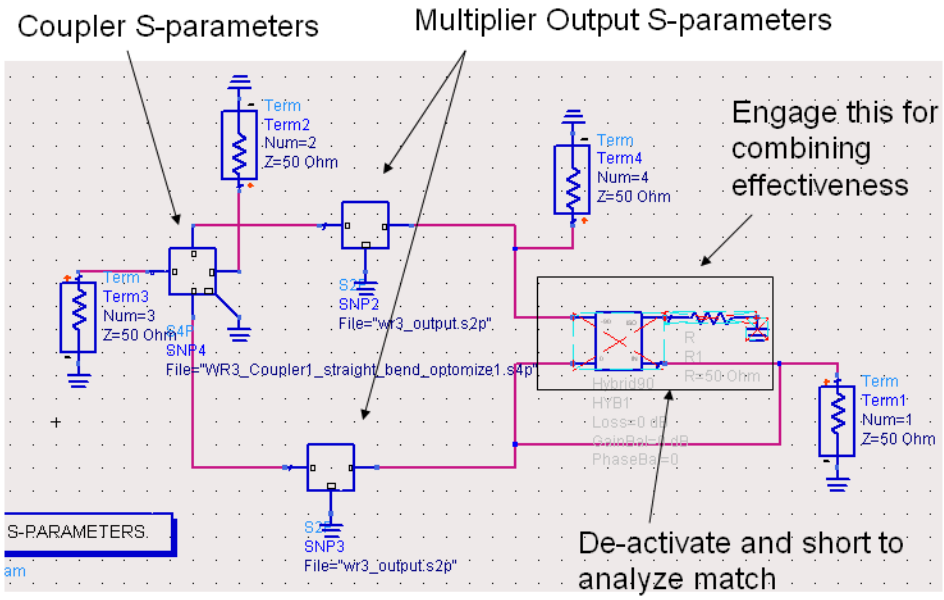

Figure 99: The ADS schematic for evaluating the output power combining for the composite circuit of the WR-3 couple and multiplier output.

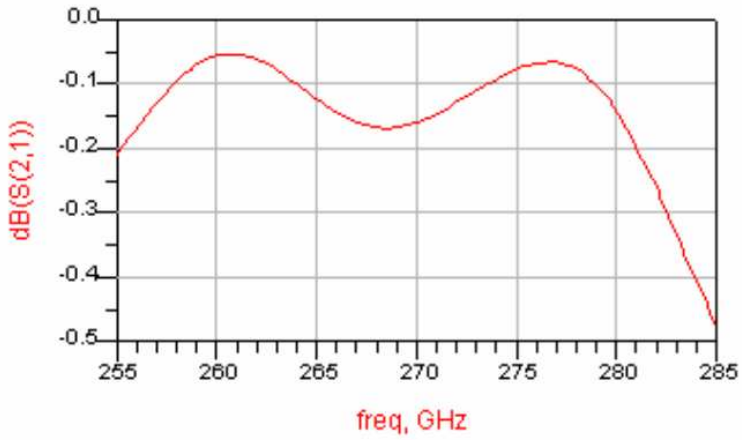

Figure 100: The simulated results of the power combining of the WR-3 coupler with two multiplier outputs attached.

To examine how well the coupler impedance match comparing to that of a single multiplier, the ideal coupler in ADS is deactivated and short circuited. The simulated results in comparison with a single multiplier are shown in Figure 102. The results from the coupler combined with the multipliers show a good agreement with the single multiplier.

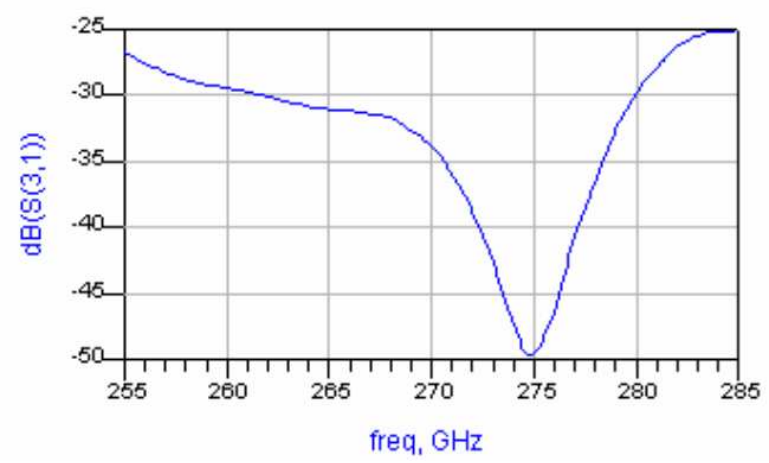

Figure 101: The simulated results of the isolation between the input and isolation port of the designed WR-3 waveguide.

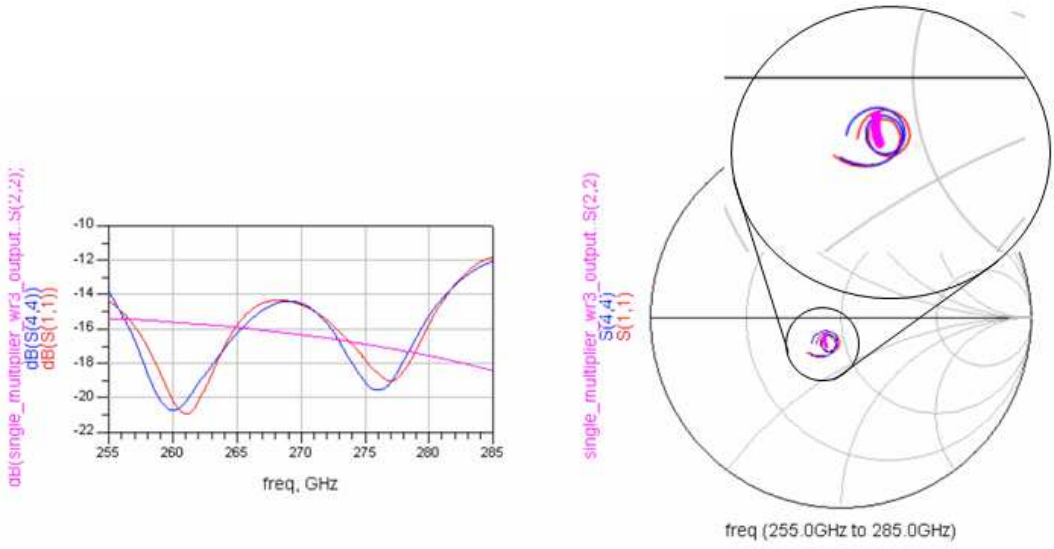

Figure 102: The simulated results of the impedance match of the WR-3 coupler and out put multiplier section at the microstrip port compared to a single multiplier.

5.7 Fabrication

Throughout this dissertation, silicon micromachined waveguide has been presented and verified to be a viable alternative to traditional metal waveguide. The method of fabrication utilized in the single multiplier requires multiple wafers due to the lack of multiple depth control using DRIE (see Figure 50).

However, the branchline coupler is a more complicated structure, and this type of fabrication method can not be utilized. The reason is as follows: when the middle wafers are

fabricated, the posts for the coupler branches do not have an attachment point to the rest of the wafer and will simply be etched away.

One half of the coupler section is shown in Figure 103.

The section shown in Figure 103 needs to be formed with three wafers to form the necessary depths of the other section of the circuit as with the single multiplier (see Figure 50. Clearly the coupler posts would be etched away in the second and third wafer for each half of the assembly. An alternative to continue to utilize silicon micromachining would be by laser etching [60]. This method can handle the multiple etch depths, and thus, two wafers can be used for the fabrication, each one of them used for one half of the branch line couplers. An example of the depth control of the silicon laser etch system is shown in Figure 104 [50]. Unfortunately, the laser etch system is not available in the research institute and is not an option at the present time.

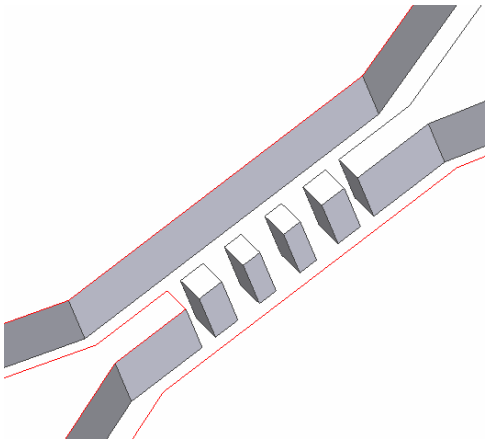

Figure 103: A closer view of the branch section of the WR-3 branchline coupler.

Thus, in this section, the author focuses on addressing the concept, and the brass block waveguide is manufactured. The layout of the entire structure is shown in Figure 105. The majority of the block is machined using standard milling techniques with the exception of the branches of the branchline couplers. The smaller dimensions of the coupler branch require a technology called electrical discharge machining (or EDM). EDM is a nontraditional method, that removes material by a series of rapidly recurring electric arcing discharges between an electrode (the cutting tool) and the work piece, in the presence of an energetic electric field.The EDM cutting tool is then guided along the desired path very close to

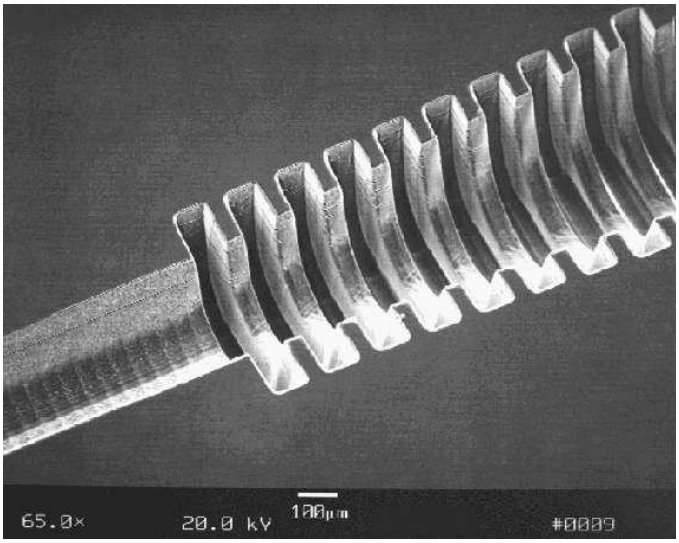

Figure 104: An example of the capability of a silicon laser etching system. An 810 GHz feedhorn is shown.

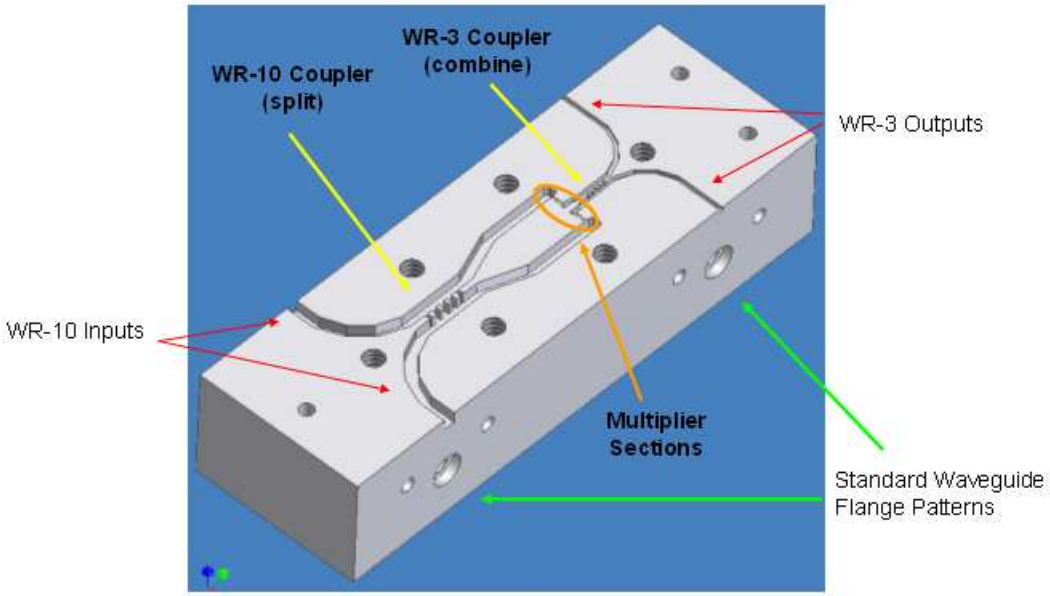

Figure 105: A complete layout of the power combining multiplier block.

the object but does not physically touch it. Consecutive sparks produce a series of micro-craters on the work piece and remove material along the cutting path by melting and vaporization. The particles are washed away by the continuously flushing dielectric fluid [68]. The fabricated final combiner is shown in Figure 106. A close of view of the combiner with the diodes circuits installed is shown in Figure 107.

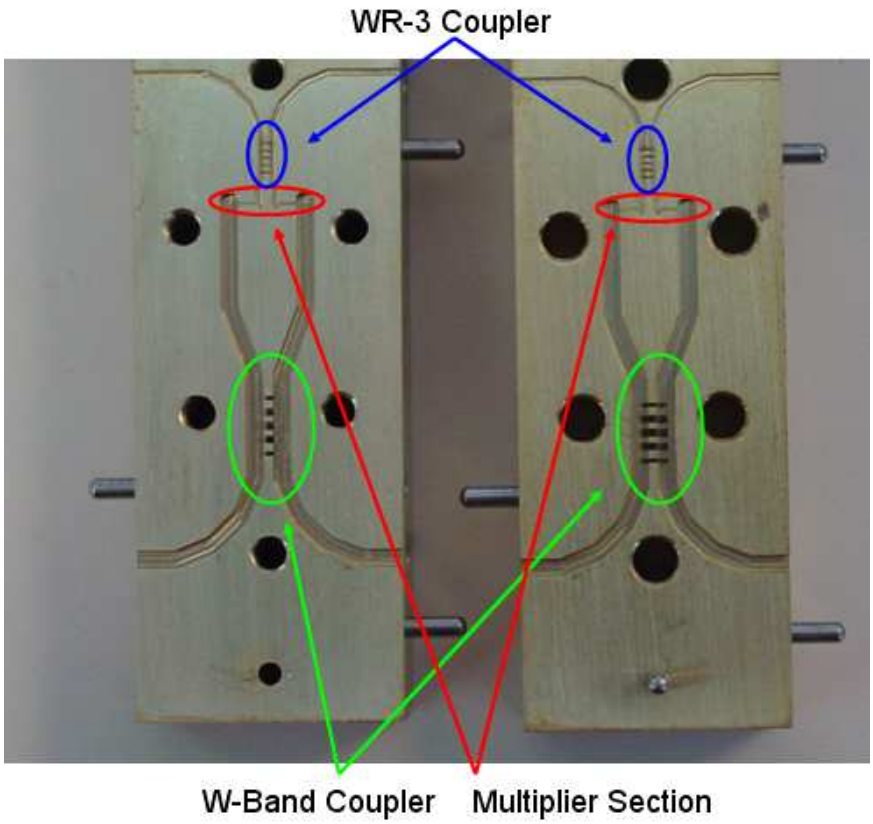

Figure 106: The fabricated final power combiner block.

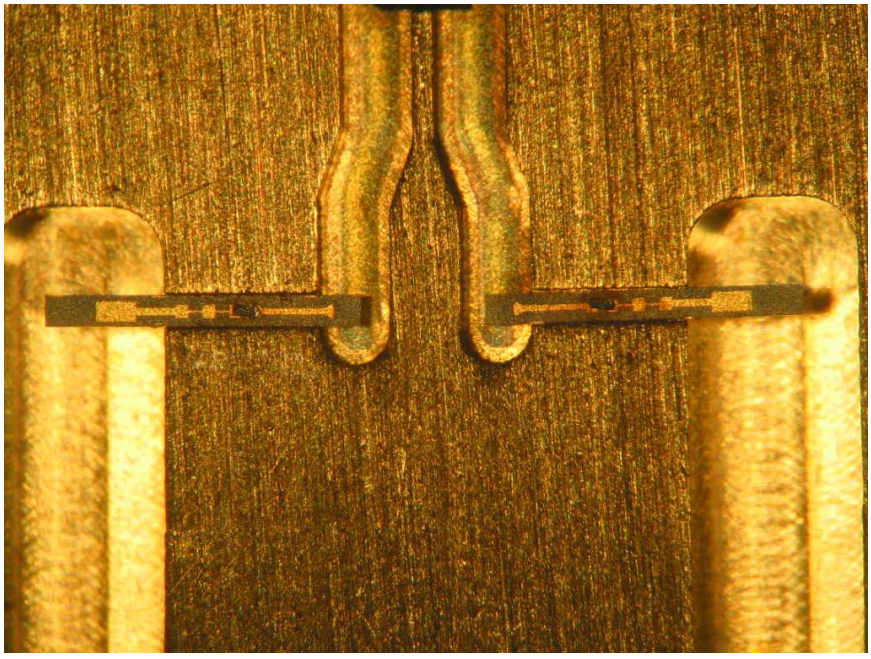

Figure 107: A close-up view of the final power combiner with the diode circuits installed.

5.8 Measurement

The measurement of the the power combiner block is very similar to the measurement of the the single multiplier discussed in section 4.4. The measurement was done at the University of Virginia in conjunction with Virginia Diodes, Inc. However, the desired output power of the multiplier chain of 200 mW (or input power to the combiner block) was not attainable with the available equipment. An attempt was made to minimize components in the multiplier chain to increase the output power. Two photographs of the measurement setup are shown in Figure 108 and Figure 109. The frequency is initiated in the setup by an Agilent E8247C

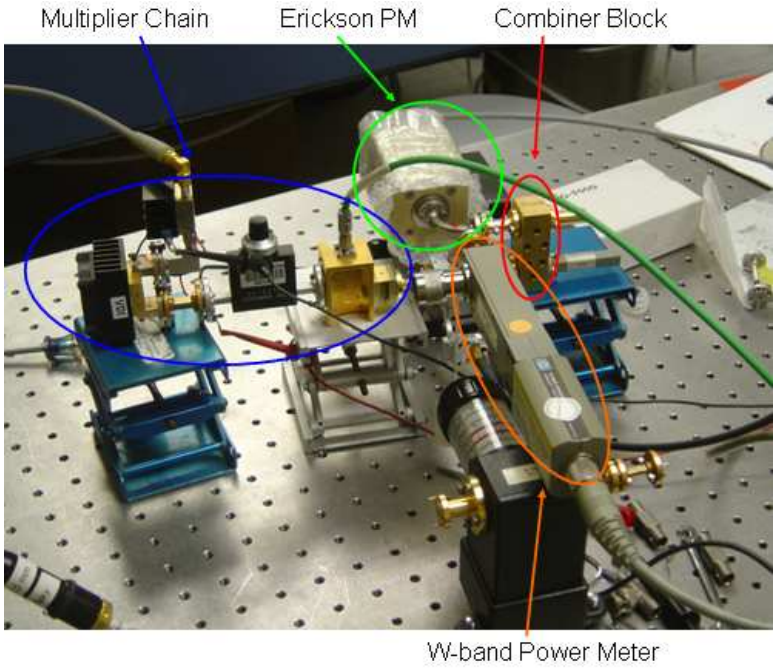

Figure 108: The sideview photograph of the measurement for the power combiner block characterization.

Signal Generator, which provides a source signal from 10.5 to 11.17 GHz. The source is then fed into a Spacek Labs amplifier to provide a high drive level for the Spacek quadrupler, which multipies the frequency to the range of 43.5 to 46.5 Following the output of the quadrupler is WR-19 waveguide variable attenuator. This attenuator helps to control the drive level, if necessary, to the next multiplier.The final multiplier is a D-90 doubler from Virginia Diodes, Inc., the input is WR-19 waveguide and the output is WR-10 waveguide. To maintain a good impedance match, an isolator is attached to the output of this doubler.

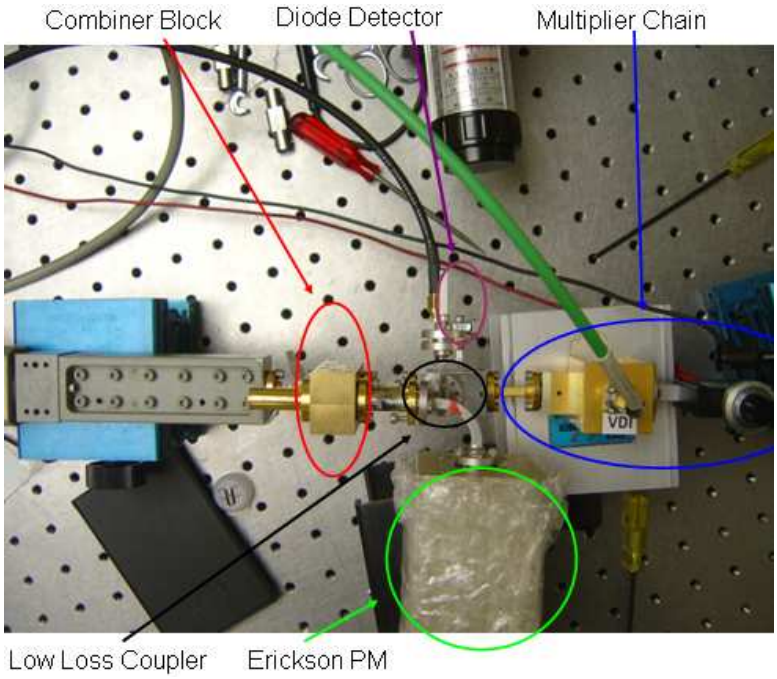

Figure 109: A top view photograph of the measurement setup to characterize the combiner block.

Originally, the output was fed through a WR-10 variable attenuator; this was removed to reduce losses and the output power will be controlled by the WR-19 variable attenuator. The following component is an Erickson WR-10 4 port coupler. The reflection port of the coupler is utilized to characterize the reflected power from the DUT via a diode detector. The final two components are an Erickson power meter for measuring the output power of the combiner block and an Agilent W-Band power sensor for measuring the input power to the combiner block.

As previously mentioned, the output power of the multiplier chain at W-Band is limited. The desired power level for each of the two diode circuits is approximately 100 mW, which equates to a total input signal power of 200 mW in an ideal case. The measured output power at the W-band port is shown in Figure 110. Additionally, Figure 110 also shows one-half of the input power which ideally is the power available to each diode, if the input power split equally without any losses.

The measurements are made over an output frequency range of 252-268 GHz, corresponding to an input frequency range of 84-89.3 GHz. The measured output power versus

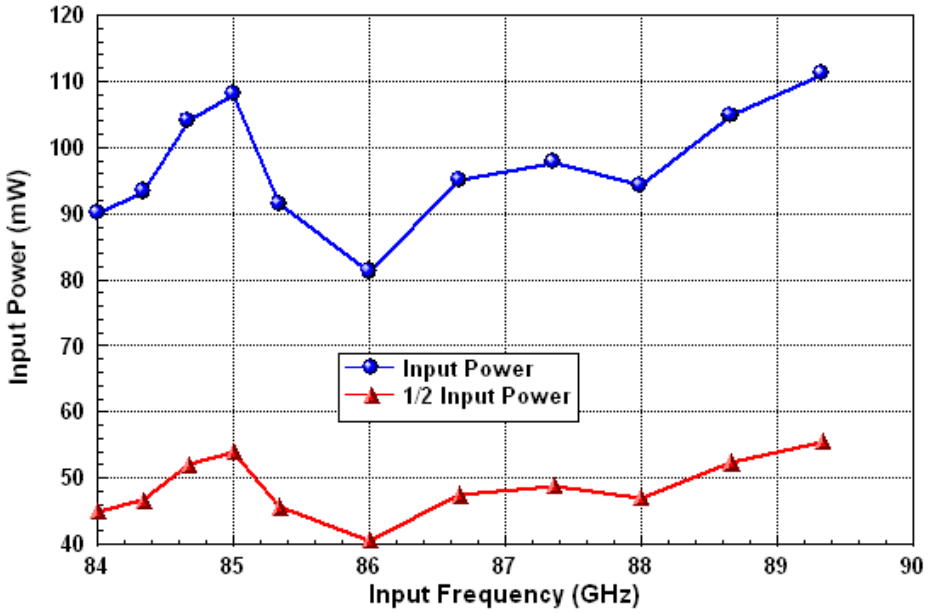

Figure 110: The available to the input of the combiner generated by the multiplier chain. The one-half power is the ideal amount of power available to each diode circuit.

the input power to the power combiner is shown in Figure 111.The measured efficiency is

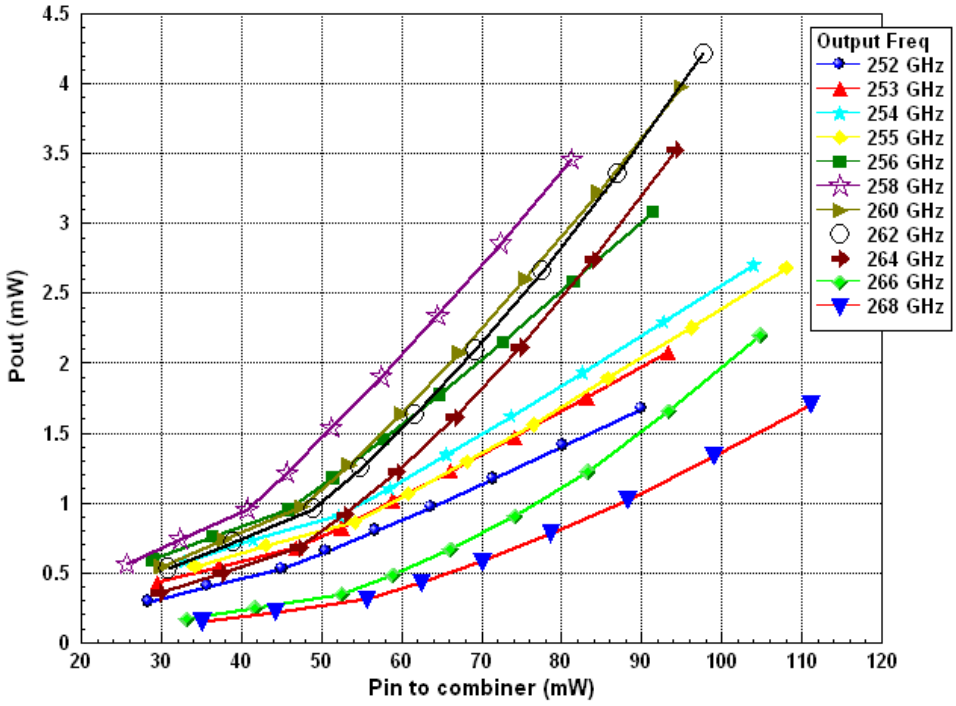

Figure 111: The output power versus input power of the power combiner block.

shown in Figure 112. It can be seen in Figure 112 that both the maximum output power

and maximum efficiency occurs at an output frequency of 262 GHz. The bandwidth of the power combiner is shown in Figure 113, where the values plotted are shown for the maximum input power available for each frequency point.

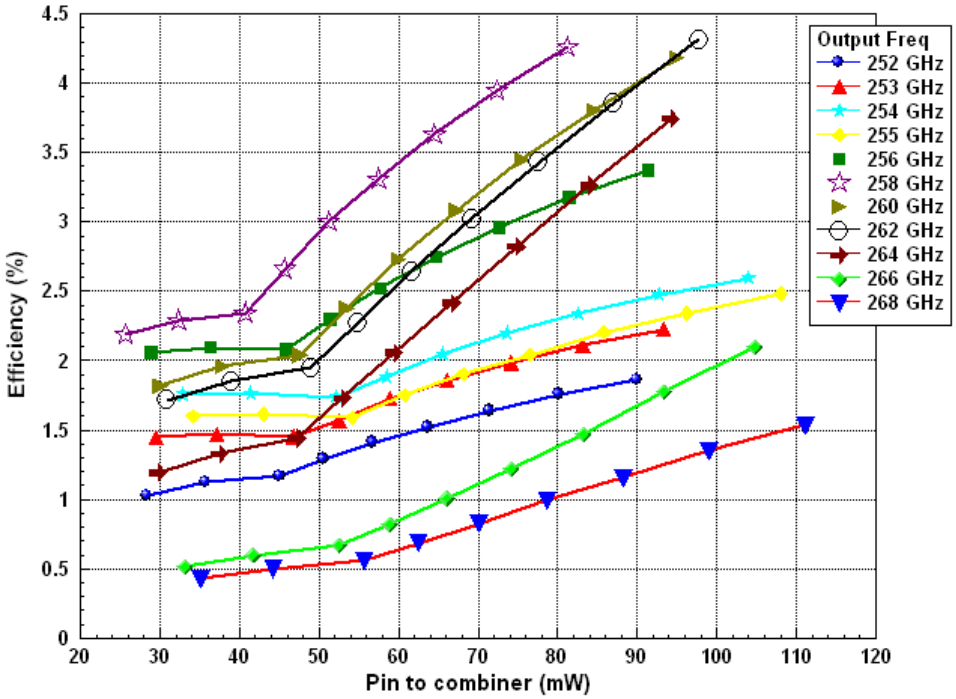

Figure 112: Conversion efficiency versus input power of the power combiner block.

To evaluate the performance of the power combiner, a single diode circuit is installed into a single multiplier fixture which has a similar frequency response to that of the power combiner. The performance of the single multiplier is shown in Figure 114. For a better comparison, the output power of the single multiplier at the corresponding maximum one-half input power to the combiner (in Figure 110) is doubled and compared to that combiner output power. The results are summarized in Table 5.

5.9 Summary

In this chapter the method of generating higher output power using two HBV diode circuits is discussed. An ideal analysis is performed for splitting the input power and a similar analysis is performed for recombining the output power. The best option concluded is to adopt a power splitter/combiner with isolation between the two splitting branches and the two

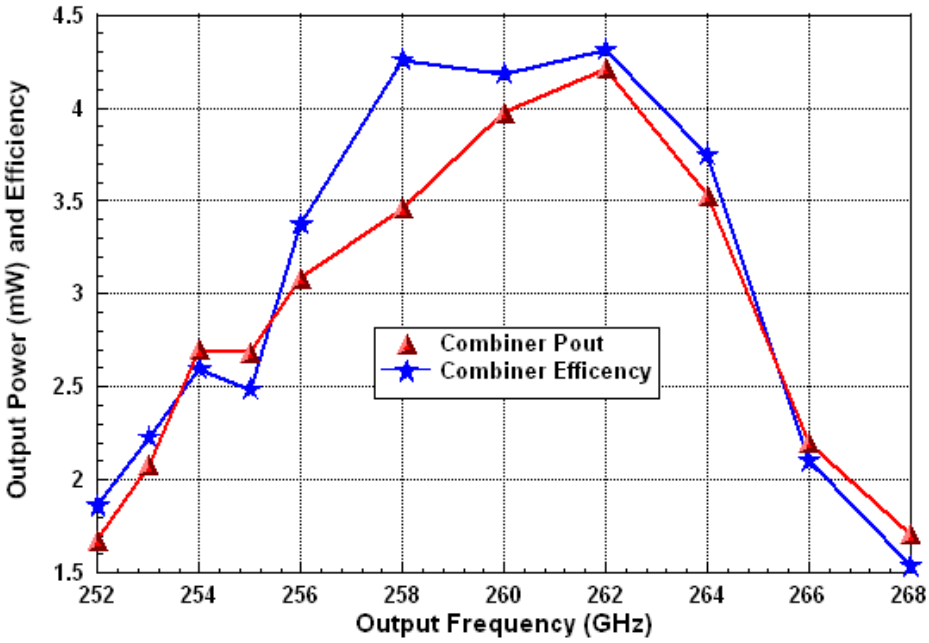

Figure 113: The output power and efficiency versus input power of the combiner block at the maximum output power for each frequency.

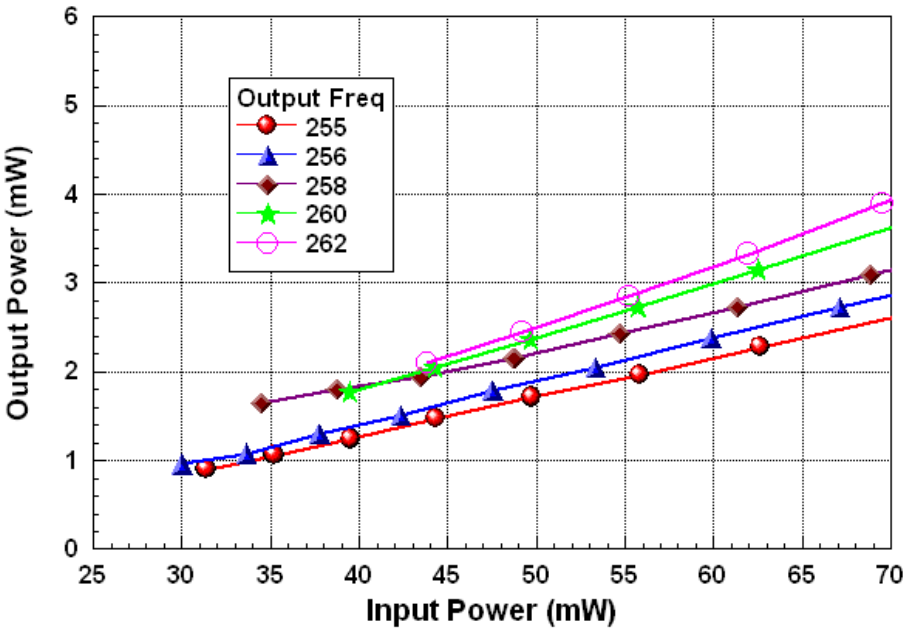

Figure 114: The output power versus input power of a single diode circuit.

combining branches. To accomplish this, two branchline waveguide couplers are developed in WR-10 and WR-3 waveguides, to accommodate the input and output waveguide size,

Table 5: A comparison of the output power of the power combiner and the output power of a single multiplier doubled. TIP = the input power to combiner; ISM = one half of the TIP, the ideal input power to single multiplier; SM= the output power of a single multiplier at an input of ISM; SMx2 = single multiplier output power doubled, Comb = the power combiner output power at an input power of TIP; and Diff = the difference in the output power between the SMx2 and the Comb.

Output Freq (GHz)	TIP(mW)	ISM (mW)	SM (mW)	SMx2 (mW)	Comb (mW)	Diff (dB)
256	91.4	45.7	1.79	3.58	3.08	-0.653
258	81.2	40.6	1.95	3.90	3.46	-0.520
260	90.0	45.0	2.19	4.38	3.98	-0.416
262	97.8	48.9	2.34	4.68	4.20	-0.470

respectively. Because of the complexity of the design, the silicon micromachining technique is not an option in the research institute at the present time, thus; a solid brass block construction is utilized. The performance of the power combiner block is evaluated and compared to that of a single block multiplier. The results show a comparable performance between the two, which proves the technique has good power generating characteristics.

CHAPTER VI

CONCLUSION

The investigation of new materials and methods for millimeter and submillimeter wave signal generation has been performed. The first portion of the research focuses on the development of the first W-band oscillator on an MHEMT substrate. An output power of 1.5 dBm is achieved with a phase noise of -101 dBc/Hz at a 1 MHz offset. A unique technique has been developed for injection locking an oscillator for phase noise characterization. The comparison of this oscillator to the state of the art showed excellent performance in both the output power and the phase noise.

The second portion of this research revolves around the THz technology development. The initial step is the development of the straight section of silicon micromachined rectangular waveguide at 400 GHz. The significant amount of work has been done toward the fabrication process and the packaging, for the characterization of the straight waveguide. The straight section has achieved a very good performance. With this success, a multiplier based on a more complicated silicon micromachined waveguide utilizing an HBV diode is successfully developed at an output frequency of 261 GHz. The design uses a stacked approach to create the multiple depths needed that is not feasible in a single wafer using a DRIE process. An improved packaging method has been developed for the performance characterization. The results has shown very little difference between using the silicon micromachined waveguide and a metal block.

The final thrust of this research is the pursuit of a higher output power utilizing the same diode circuit of the single multiplier. This is accomplished by using a branchline waveguide coupler to split the input power and, another branchline waveguide coupler to recombine the power after it is fed through two different diode circuits. Because of the complexity of the design, silicon micromachining technique has been ruled out as an alternative, as the result, the power combining block is fabricated with a solid brass block. The performance

of the power combiner block is evaluated, and the the results are compared to that of a single block multiplier. The results have showed a comparable performance and a good power generating characteristics.

CHAPTER VII

CONTRIBUTIONS

There have been many contributions to the academic and industry communities as a result of this research work. The most substantial of these contributions are as follows:

- The first W-Band oscillator on an MHEMT substrate
- A unique injection locking method for phase noise characterization
- The development of the fabrication techniques using DRIE for silicon micromachined waveguide
- The development of fixtures to allow the characterization of micromachined silicon waveguide components
- The first micromachined silicon waveguide characterized at 400 GHz
- The first micromachined silicon waveguide based frequency multiplier utilizing an HBV diode with an output frequency of 261 GHz
- The development of a power combining waveguide structure, for high output power generation utilizing two HBV diode circuits

CHAPTER VIII

PUBLICATIONS TO DATE

The following journal and conference papers have been accepted or are presently under review:

Journal Publications

- **P. L. Kirby**, D. Pukala, H. Manohara, I. Mehdi and J. Papapolymerou, "Characterization of Micromachined Silicon Rectangular Waveguide at 400 GHz," IEEE Microwave and Wireless Components Letters, pp. 366-368, June 2006.
- Y. Li, **P. L. Kirby**, O.Offranc and J. Papapolymerou, "Silicon micromachined W-band hybrid coupler, power divider/combiner," Submitted to IEEE Microwave and Wireless Components Letters

Conferences Publications

- **P. L. Kirby**, Y. Li, Q. Xiao, J. L. Hesler and J. Papapolymerou, "Silicon Micromachined Multiplier Utilizing Heterostructure Barrier Varactor Diode," 2007 IEEE International Microwave Symposium, pp. 1141-1144, Honolulu, HI, June 2007.
- Y. Li, **P. L. Kirby** and J. Papapolymerou, "Silicon Micromachined W-Band Bandpass Filter Using DRIE Technique," 36th European Microwave Conference, pp. 1271 - 1273, Manchester, UK, September 2006.
- **P. L. Kirby**, K. Herrick, R. Alm, N. A. Luque, A. Rodriguez, L. P. Dunleavy, J. Papapolymerou, "W-Band Oscillator on Metamorphic HEMT," 2006 IEEE International Microwave Symposium, pp. 735-738, San Francisco, CA, June 2006.
- Y. Li, **P. L. Kirby** and J. Papapolymerou, "Silicon Micromachined W-Band Folded and Straight Waveguides Using DRIE Technique," 2006 IEEE International Microwave Symposium, pp. 1915 - 1918, San Francisco, CA, June 2006

- **P. L. Kirby** and J. Papapolymerou, "Micromachined Si Waveguides for THz Applications," URSI National Radio Science Meeting, Boulder, Colorado, January 2005.

- N.D. Kingsley, **P. L. Kirby**, G. Ponchak, and J. Papapolymerou, "14GHz MEMS 4-bit Phase Shifter on Silicon," 2004 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 326-328, Atlanta, Georgia, September 2004.

- G. Zheng, **P. L. Kirby**, S. Pajic, J. Papapolymerou, and Z. Popovic, "A Monolithic Reconfigurable Tuner with Ohmic Contact MEMS Switches for Efficiency Optimization of X-band Power Amplifiers," 2004 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 159-162, Atlanta, Georgia, September 2004.

- **P. L. Kirby**, D. Pukala, H. Manohara, I. Mehdi, J. Papapolymerou, "A micromachined 400 GHz rectangular waveguide and 3-pole bandpass filter on a silicon substrate," 2004 IEEE MTT-S International Microwave Symposium Digest, pp. 1185-1188, Fort-Worth, Texas, June 2004.

- B. Pan, Y. Yoon, **P. Kirby**, J. Papapolymerou, M. M. Tentzeris and M. Allen, "A W-band Surface Micromachined Monopole for Low-cost Wireless Communication Systems," 2004 IEEE MTT-S International Microwave Symposium Digest, pp.1935-1938, Fort-Worth, Texas, June 2004

- Y.-K. Yoon, B. Pan, **P. Kirby**, J. Papapolymerou, M. Tentzeris, and M.G. Allen, "Surface micromachined Electromagnetically radiating RF MEMS," Digest of Solid-State Sensor, Actuator,and Microsystems Workshop 2004, pp. 328-331, Hilton Head Island, South Carolina, June 2004.

- G. Zheng, **P. Kirby**, A. Rodriguez, J. Papapolymerou, M. Tentzeris, and L. Dunleavy, "Design and On-Wafer Measurement of a W-Band Via-Less CPW to Microstrip Transition," 2003 European Microwave Conference, pp. 443-446, Munich, Germany, October 2003.

- D. Thompson, **P. Kirby**, J. Papapolymerou, and M. M. Tentzeris, "W-band characterization of finite ground coplanar transmission lines on liquid crystal polymer

(LCP) substrates," IEEE Electronic Components and Technology Conference, pp. 1652-1655, New Orleans, Louisiana, May 2003.

- **P. Kirby**, J. Papapolymerou, C. D Aubigny and C. Walker , "Silicon Laser Micromachining for the Development of Planar Waveguide-Based THz Structures," Fourteenth International Symposium Space TeraHertz Technology, Tuscon, AZ, April 2003.

- **P. Kirby**, V. lliopoulos, J. Papapolymerou, C. D' Aubigny and C.Walker, "Silicon Micromachining for the Development of Planar Waveguide-Based Structures from a Few GHz to a Few THz," 2003 Progress in Electromagnetics Research Symposium, Singapore, January 2003.

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